

OPEN-ISA.ORG, RV32M1, VEGABOARD & SDK

OVERVIEW



PUBLIC



SECURE CONNECTIONS
FOR A SMARTER WORLD

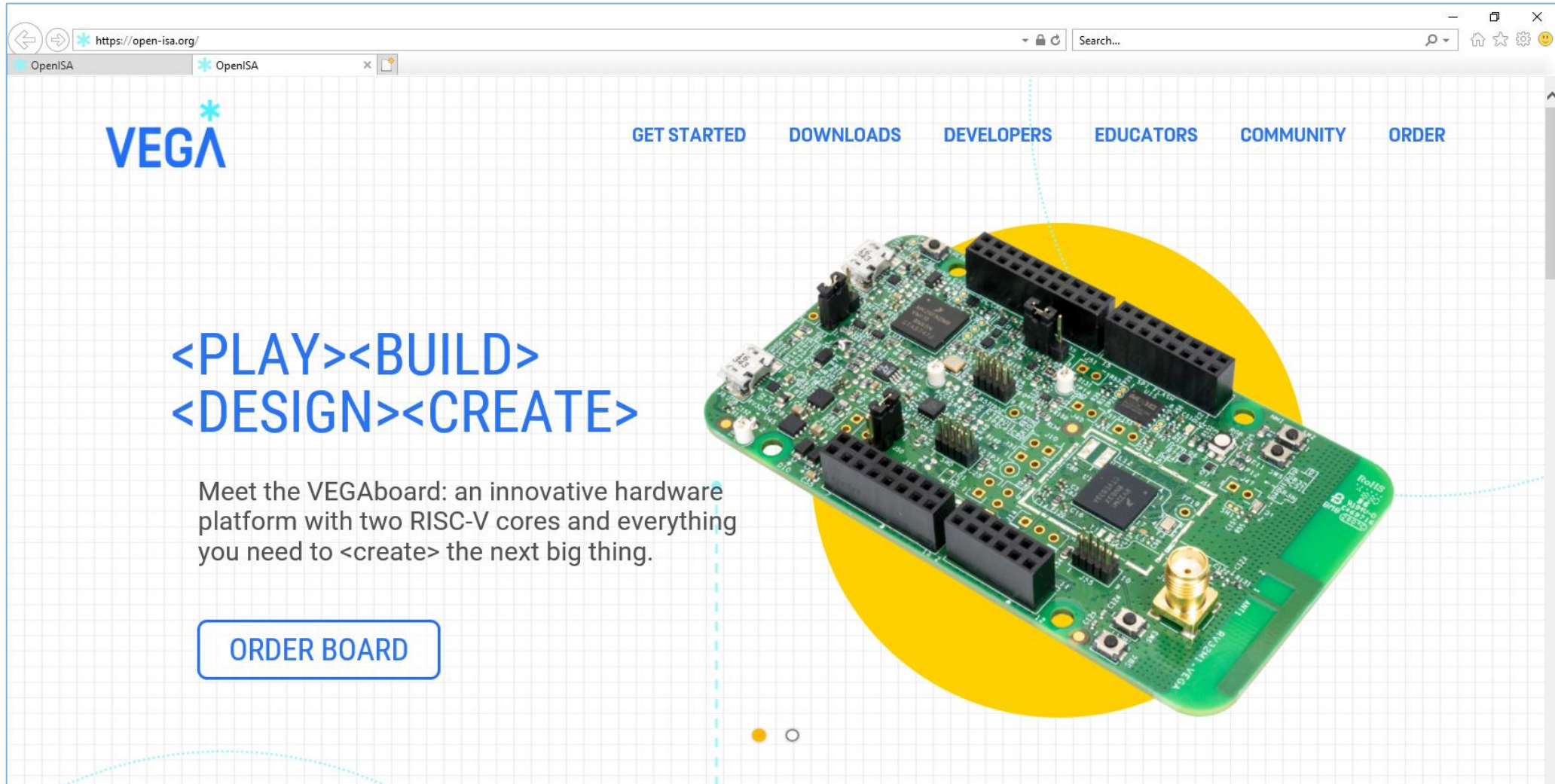
Agenda

- www.open-isa.org
- RV32M1 SoC
- VEGAboard
- VEGAboard SDK

www.open-isa.org

- One site for all Open-source ISA enthusiasts
- Open-ISA's Role → Expand RISC-V Ecosystem
- Open to any and all relevant ecosystem partners
- Developers sharing ideas & experiences
- Discussion board
- Order VEGAboard & download documentation

Join the [Open-ISA](http://www.open-isa.org) Community



The screenshot shows the OpenISA website homepage. At the top left is the VEGA logo, which consists of the word "VEGA" in blue with a small blue asterisk above the "A". To the right of the logo is a navigation bar with the following links: "GET STARTED", "DOWNLOADS", "DEVELOPERS", "EDUCATORS", "COMMUNITY", and "ORDER". Below the navigation bar, on the left, is the text "<PLAY><BUILD><DESIGN><CREATE>" in blue. To the right of this text is a photograph of a green VEGAboard, a hardware platform with two RISC-V cores, various connectors, and a yellow circular highlight behind it. Below the text, there is a blue button labeled "ORDER BOARD". The website is displayed in a browser window with the address bar showing "https://open-isa.org/" and two tabs labeled "OpenISA".

VEGA

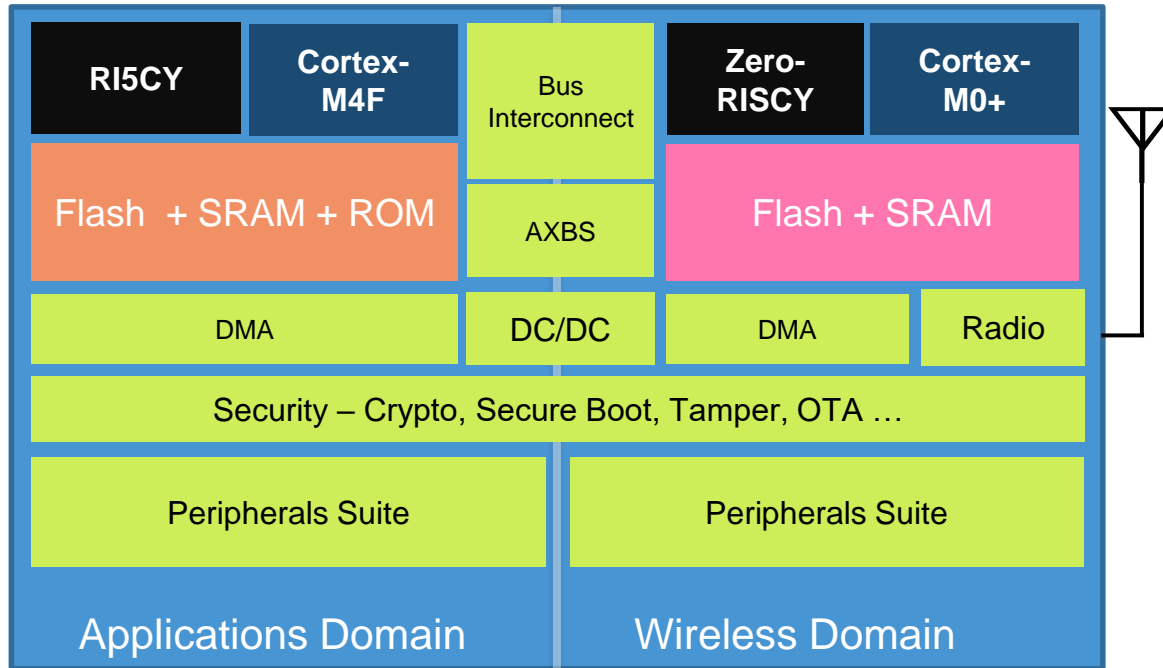
GET STARTED DOWNLOADS DEVELOPERS EDUCATORS COMMUNITY ORDER

<PLAY><BUILD>
<DESIGN><CREATE>

Meet the VEGAboard: an innovative hardware platform with two RISC-V cores and everything you need to <create> the next big thing.

ORDER BOARD

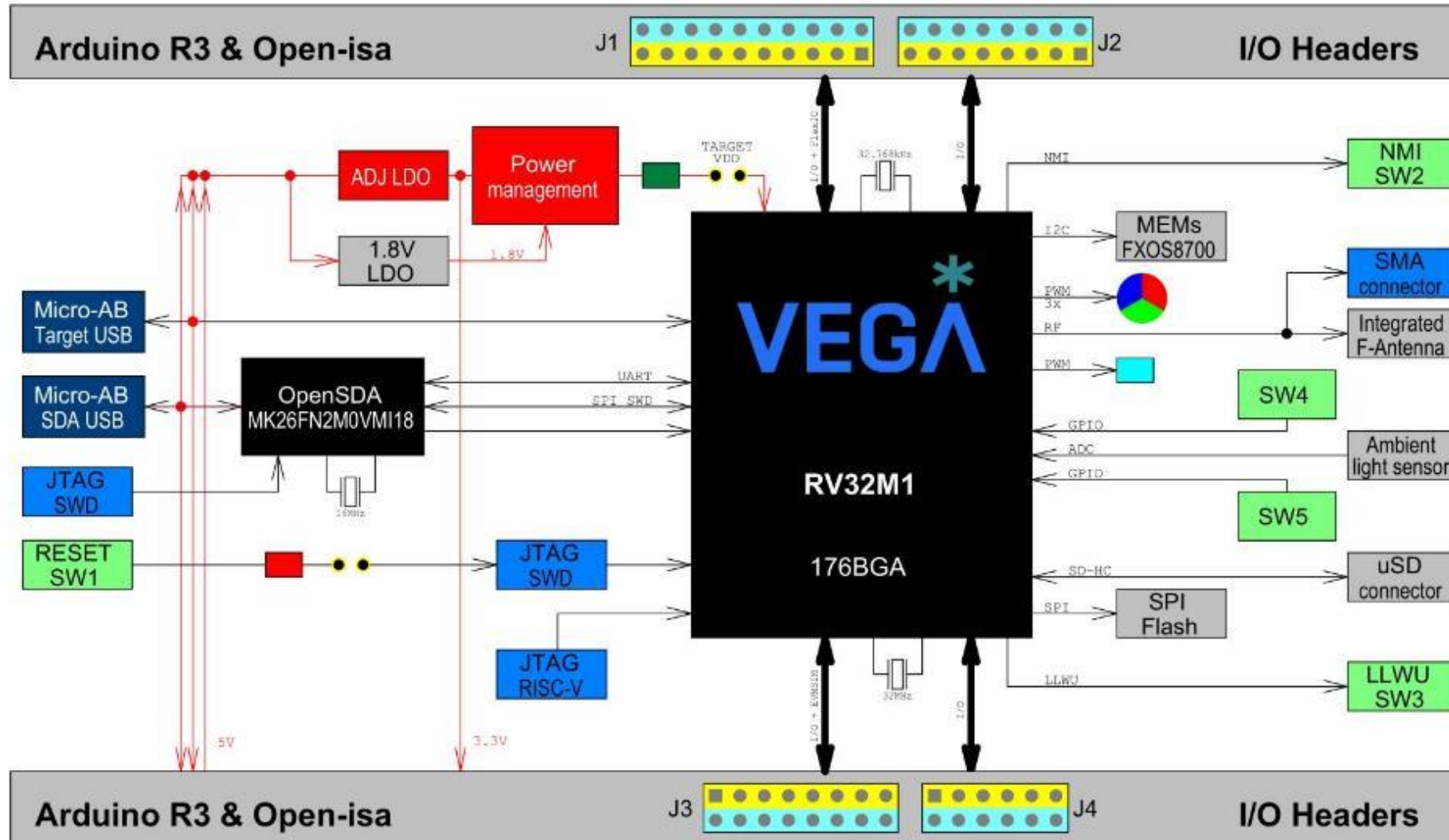
RV32M1 SOC



- Intended only as silicon evaluation vehicle
- Not for SALE!

- 4 CPU cores, up to 72MHz
 - One RISC-V RI5CY and one RISC-V ZERO_RISCY
 - One ARM Cortex-M4F and one Cortex-M0+
- Low power consumption and high integration
 - Support BLE, Generic FSK, 802.15.4
 - Security engine include AES128/196/256, DES/3DES, SHA-256, RSA and ECC PK-256/Curve25519
 - USB2.0 FS, SAI support I2S and AC'97, SDHC, EMVSIM
 - 1x32ch FlexIO, 4xUART, 4xI2C, 4x16-bit LPSPI, 1x12bit ADC
 - 2x6ch PWM, 1x2ch PWM, RTC, LPTimer
 - 1.25 MB Flash, 384 KB SRAM

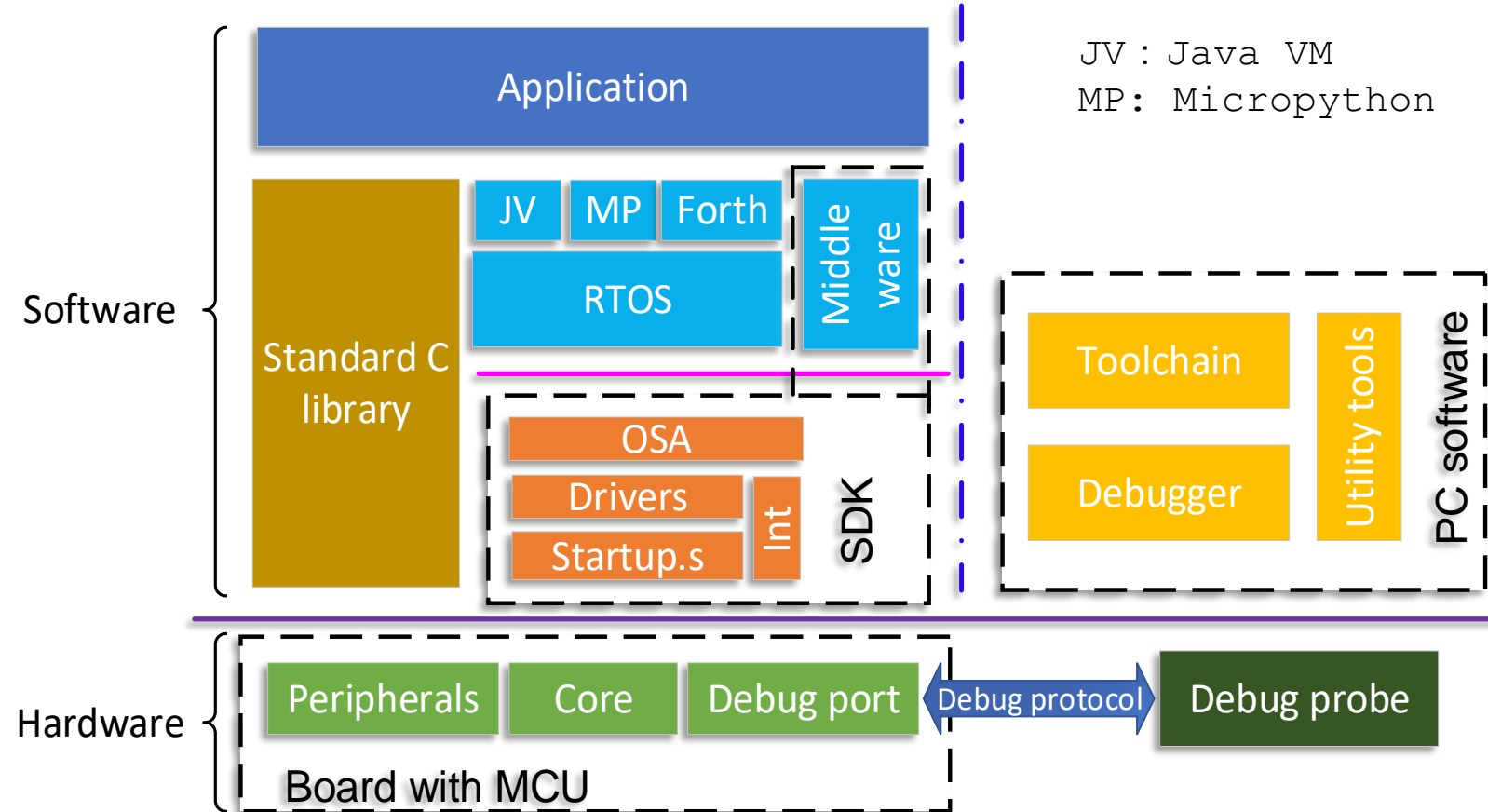
VEGAboard - Full-Featured RISC-V Secure Connected Platform



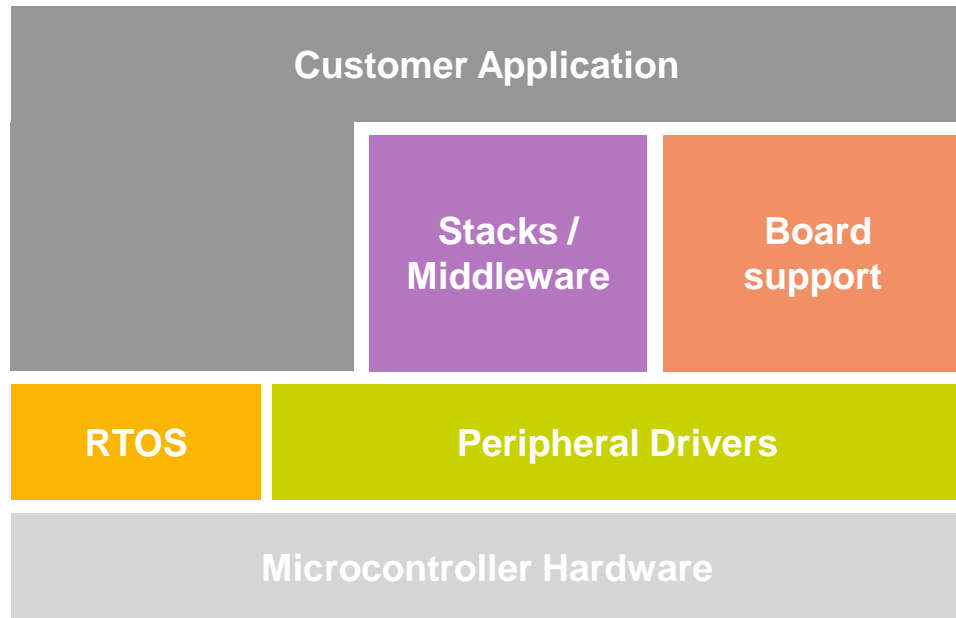
Development based on VEGAboard



- Development Tools
 - Eclipse IDE
 - GNU GCC RISC-V toolchain
 - OpenOCD debugger
- Software
 - SDK can be downloaded from OPEN-ISA website with drivers, middleware and examples
- Application development
 - Consistent with general MCU



VEGAboard SDK



Features

Architecture:

- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

Integrated RTOS:

- FreeRTOS v9
- RTOS-native driver wrappers

Integrated Stacks and Middleware

- USB Host, Device and OTG
- BLE stack
- Amazon Web Service IoT
- QCA WiFi Stacks
- lwIP, FatFS
- Crypto acceleration plus wolfSSL
- SD and eMMC card support

Reference Software:

- Peripheral driver usage examples
- Application demos
- FreeRTOS usage demos

License:

- BSD 3-clause for startup, drivers, USB stack

Toolchains:

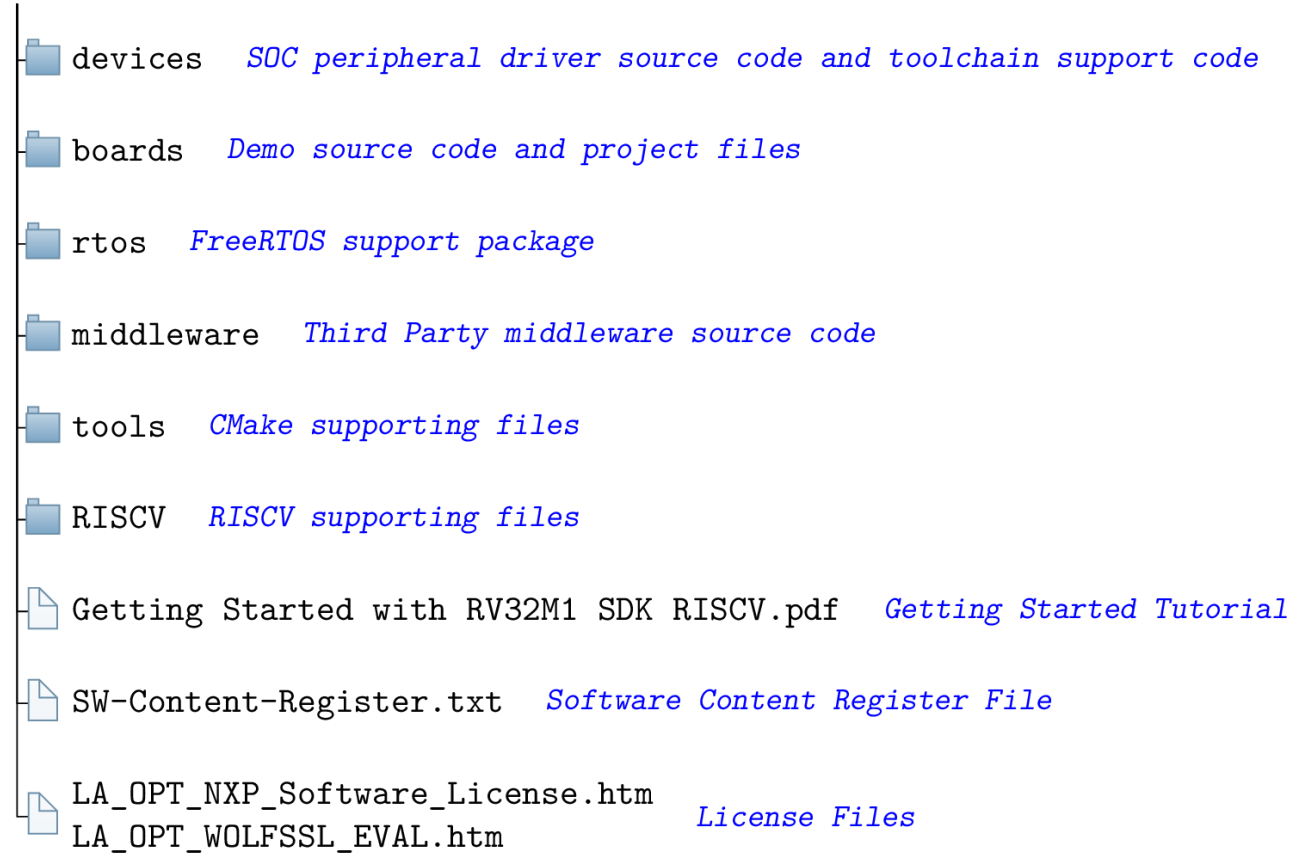
- Eclipse IDE
- GCC w/ Cmake

Quality

- Production-grade software
- MISRA 2004 compliance
- Checked with Coverity® static analysis tools

SDK Introduction – Folder Structure

<sdk root directory>



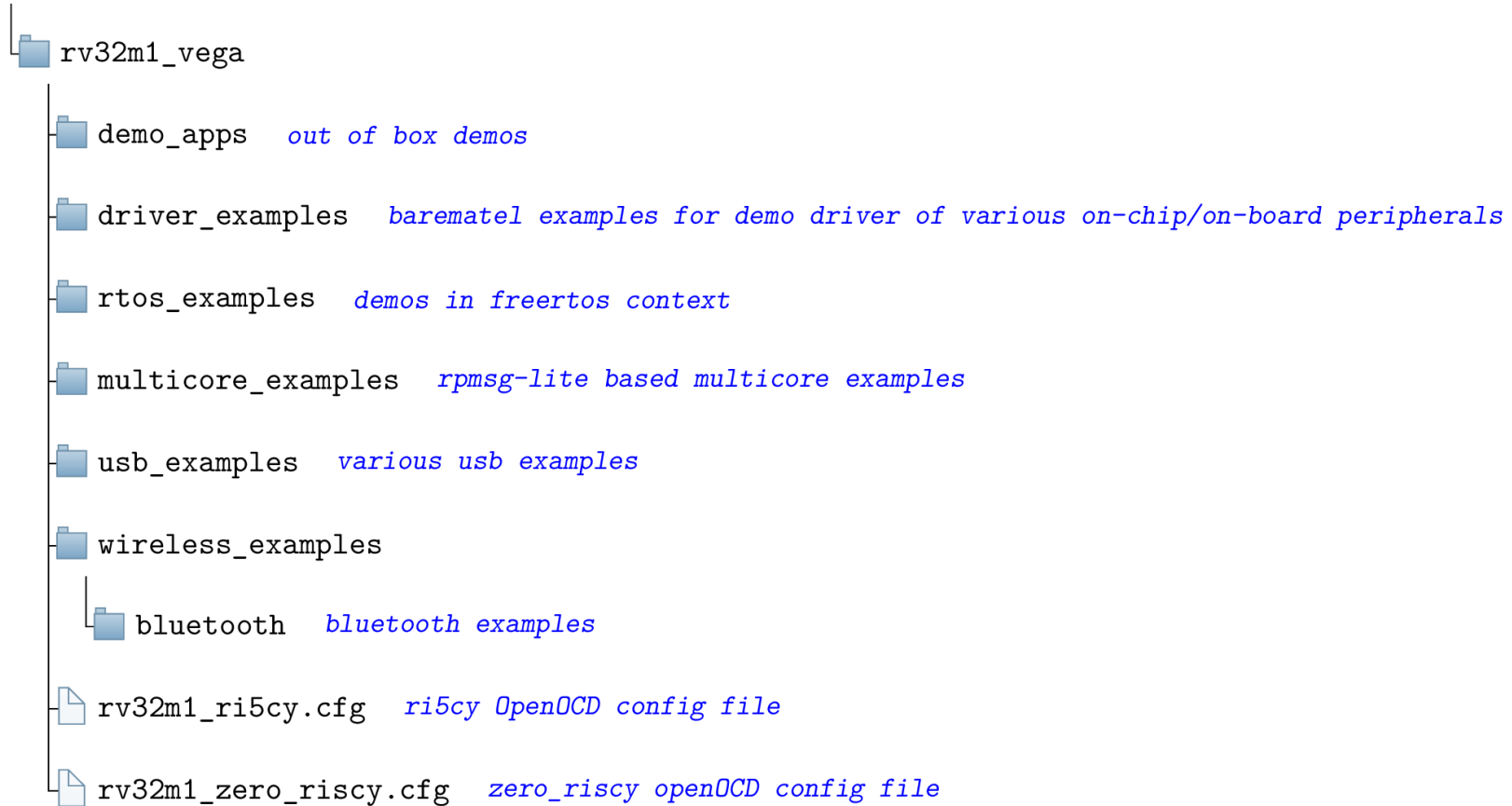
SDK Introduction – SoC Folder Structure

devices



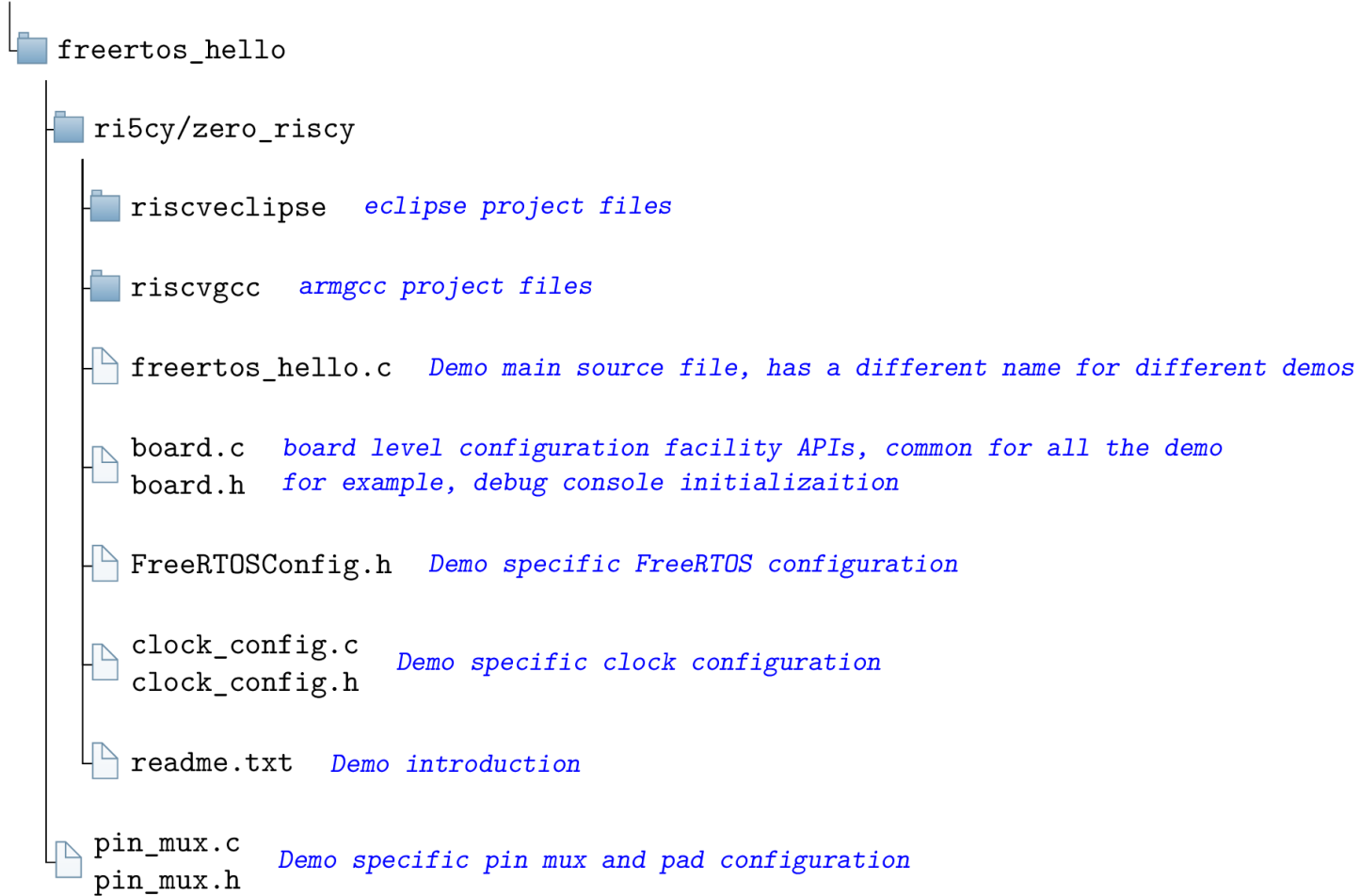
SDK Introduction – Board Folder Structure

boards



SDK Introduction – Example Folder Structure

rtos_examples





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