

A RISC-V VIRTUAL MACHINE

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 **BTA DESIGN SERVICES**
your project, our team



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Topics



- Why?
- What?
- Where? When? Who?
- How?

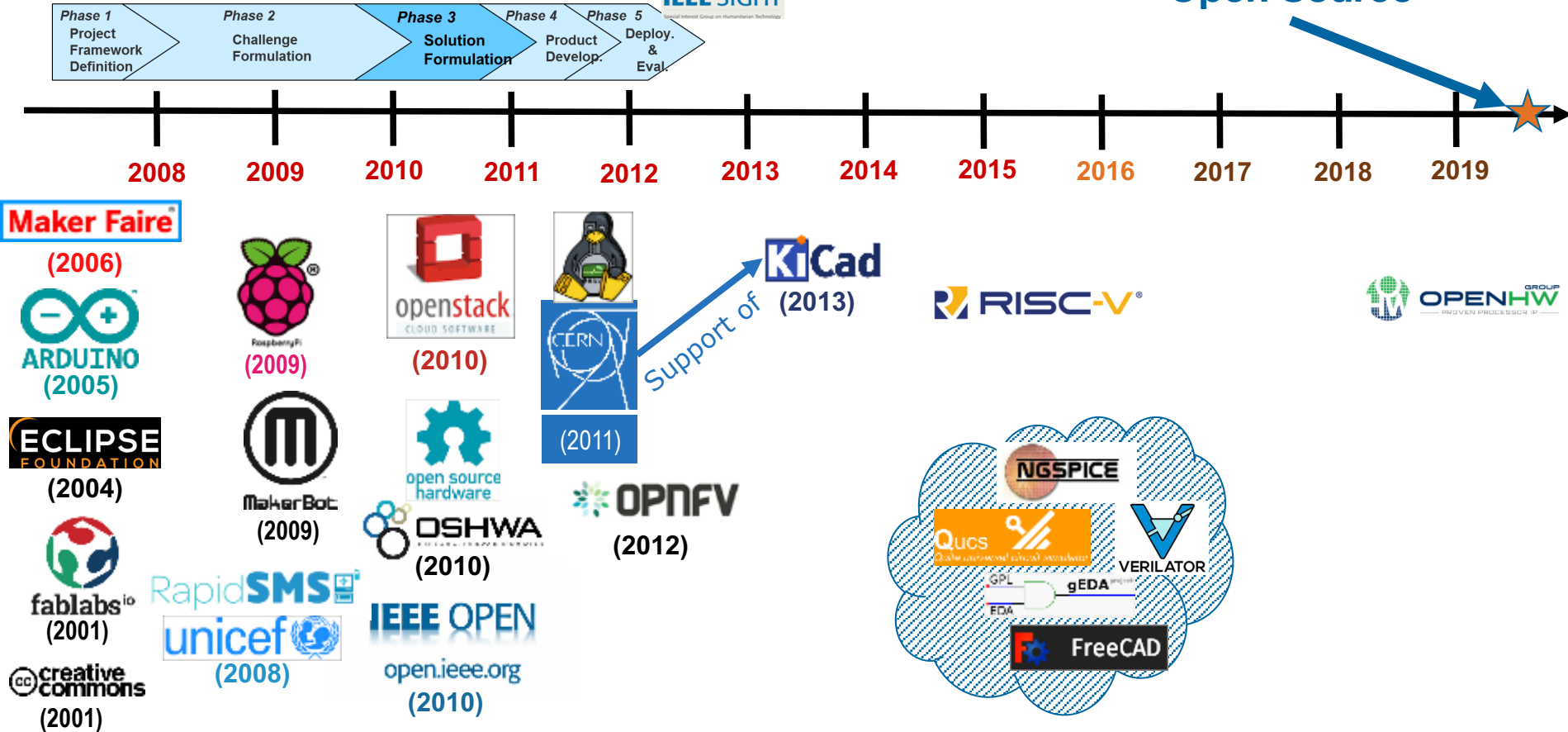


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Why create a RISC-V VM?



- Make it easier for those unfamiliar with toolchain:
 - SW toolchain: GCC/GDB, Jlink cable driver, Eclipse-IDE and Imperas fast HW model to execute SW.
 - HW toolchain: HDL simulator and cycle-accurate HW model.
- Virtual Machine pre-configured with RISC-V toolchains for anyone wanting to study, configure as-preferred, modify or physically-implement hardware.
- Permissive open source license.



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What – out of RISC-V VM scope



- Not a full-featured development environment
- Not intended to generate production ready HW
- Not bug-free
- Not supported by dedicated team
- Not guaranteed to work for you out-of-the-box (TLC required)



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What - RISC-V VM features



- Ubuntu image < 5GB 4GB RAM, 2 vCPU, 20GB dynamic HDD, USB support and toolchains:
 - PDF reader (evince), web browser (links2), X11-editor (gvim)
 - Users/Passwords: root/****, user/abc123 (sudo) -> change
 - Command-line interface to processor
 - Eclipse-IDE/OVPsim to run and debug SW
 - Verilator to run and debug functional HW and cycle-accurate HW/SW
 - Full NXP Vega board toolchain



Who, When, Where - RISC-V VM future



- BTA Design Services to continue maintenance



- Beta release at OSD forum 2019, next:
 - Release 1.0 after CENGN project completed (webinar?)
 - intermediate releases for bug fixes and improvements
 - Release 2.0 planned for OSD forum 2020



- Support of VM through:

https://github.com/openhwgroup/riscv_vm/



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