Overview of CORE-V CVE4, CVA6 & PULP Development at ETHZ

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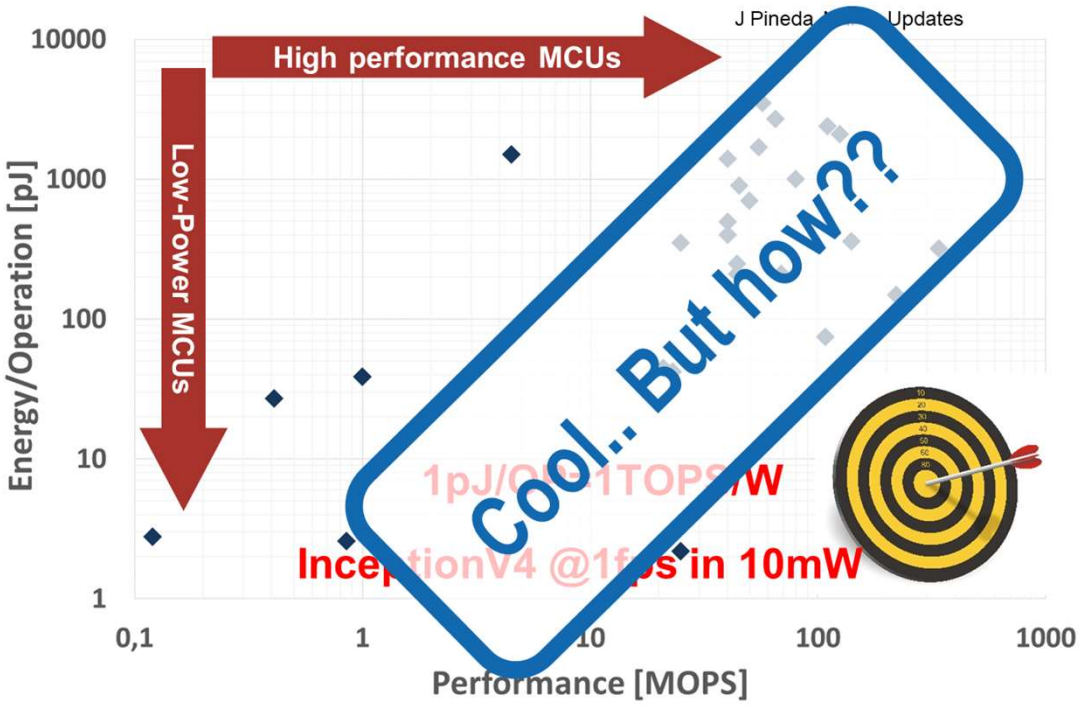
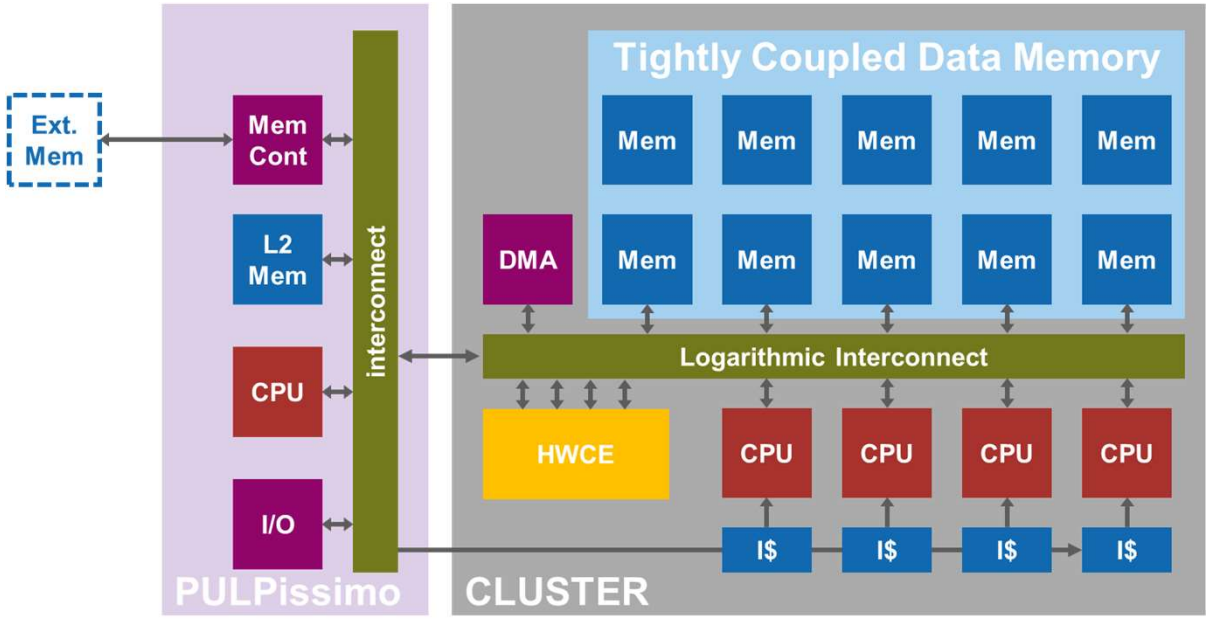
The PULP Project



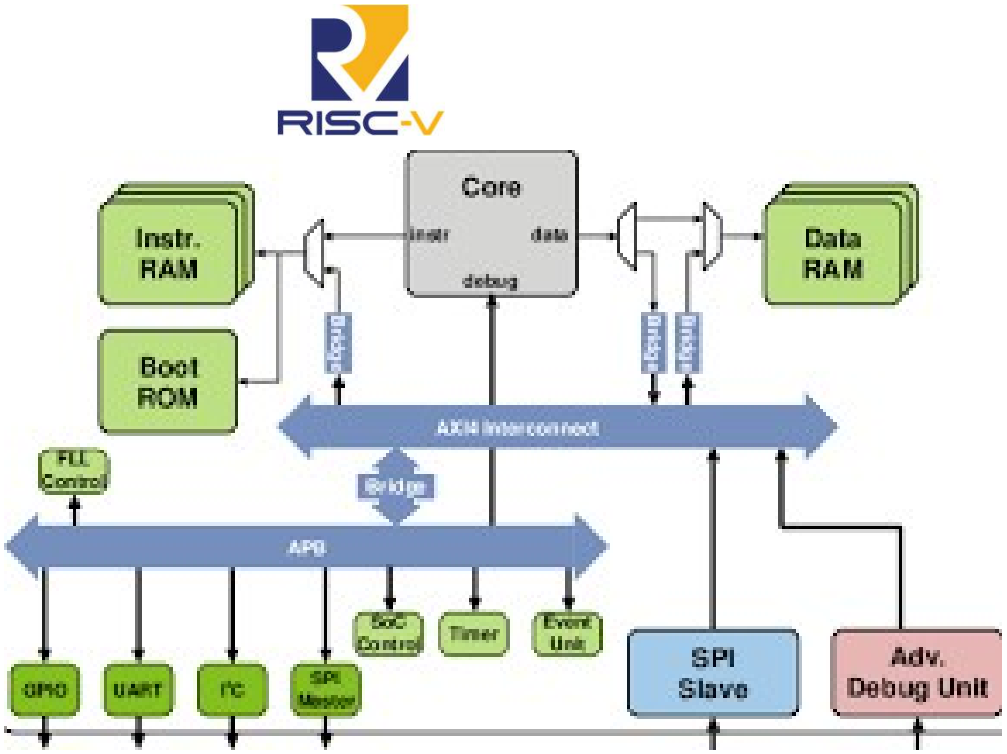
- Born in 2013 between University of Bologna and ETH Zurich
- Goal:
  - MCU with GOPS in mW power budget for Edge-Computing-Devices for the Internet-Of-Things
- How:
  - Near-Threshold-Computing and parallelization

IoT Applications and CPU Specialization



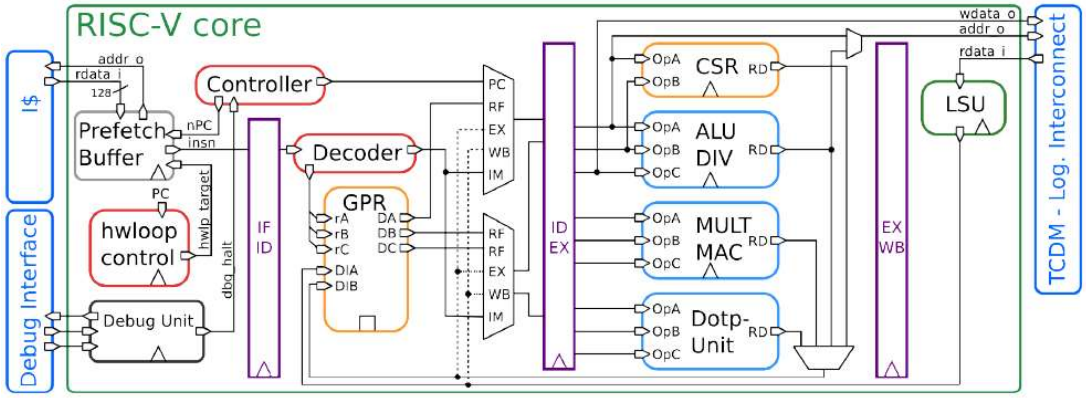
- MCU are CPU centric devices
- Edge-Computing-Devices run data-intensive algorithms
  - pattern recognition, filters, compressions
- OR10N:
  - OpenRISC ISA
  - 32b, 4-pipeline stages, in-order
  - Custom ISA extensions
    - DSP instructions
    - HW Loop
    - SIMD
    - Bit Manipulation
- Several prototypes:
  - 28nm FDSOI, UMCL 65nm

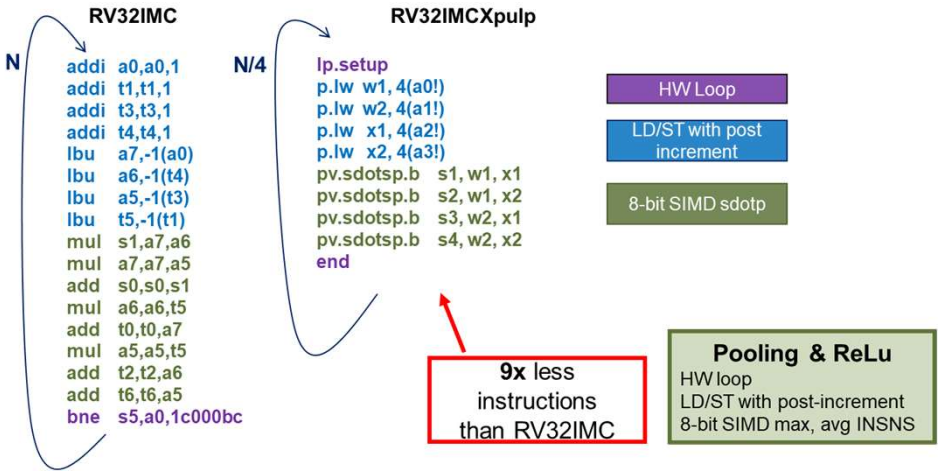
RISC-V & Open-Source



- In 2016, PULP embraces RISC-V
- RI5CY CPU as evolution of OR10N
  - Released Open-Source under SolderPad license
- PULPino:
  - Open-Source Single-Core MCU
  - Born to be a simple vehicle for the RI5CY core
- PULP GCC
  - RISC-V GCC with PULP ISA extensions
- The PULP team starts participating actively to RISC-V workshops

RI5CY

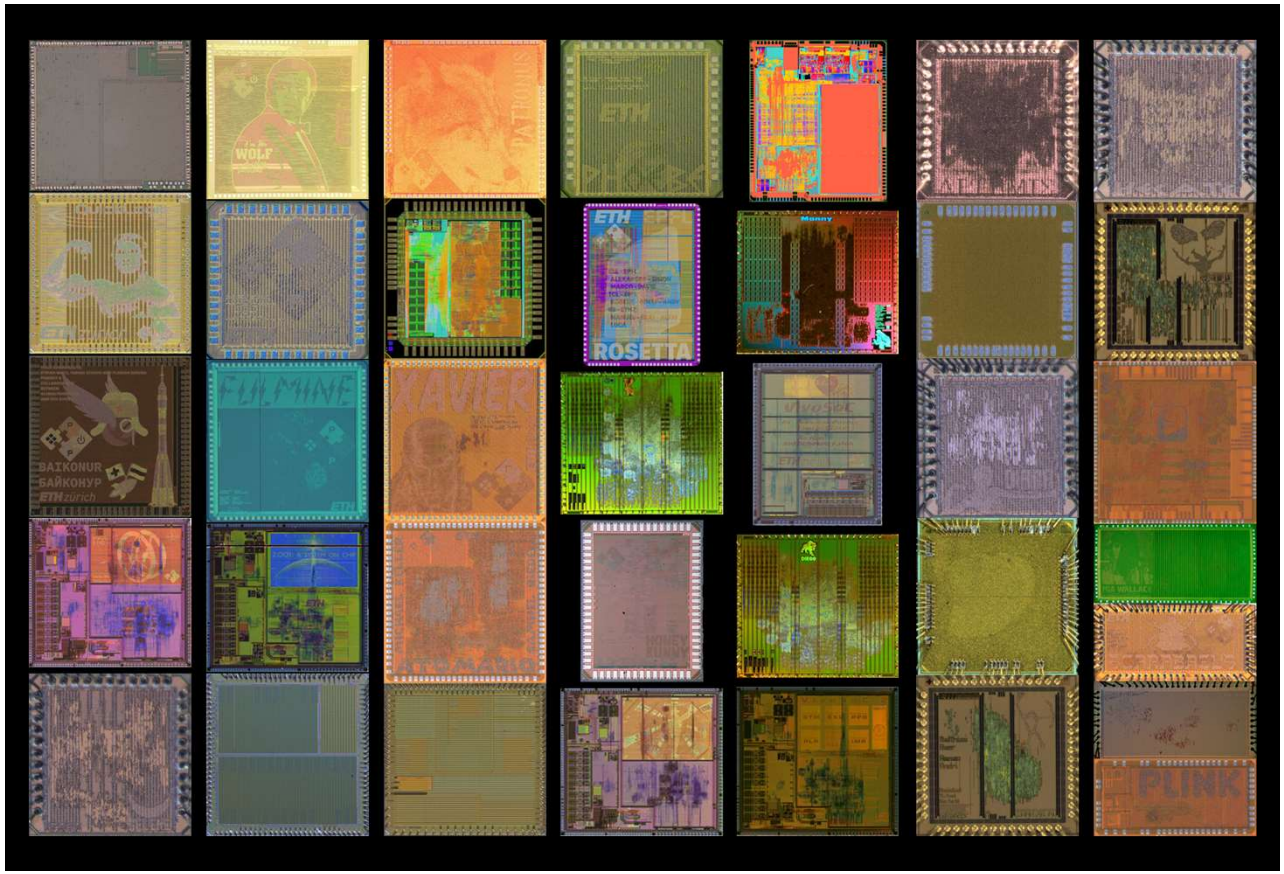




- RV32IMF[A]CXpulp
  - RISC-V Debug
- Minimal security
  - optional U privilege modes
  - Optional PMP
- 4-stage pipeline
  - In-order issue
- 600+ MHz in GF22FDX GlobalFoundries

← Very Efficiency in data-intensive algorithms (e.g. convolution)

PULP is silicon proven



- More than 37 SoCs
- Several technologies
  - 22, 28, 40, 55, 65, 110

Open-Source Facts

- Several users started using the RI5CY core
- *Embecosm* contributes for Verilator simulation
- People wrote libraries for PULPino
  - https://github.com/misaleh/CMSIS-DSP-PULPino
- Users started reporting bugs
  - Users as companies, universities, hobbyists
- Companies built products, prototypes or evaluated the core at the industrial level

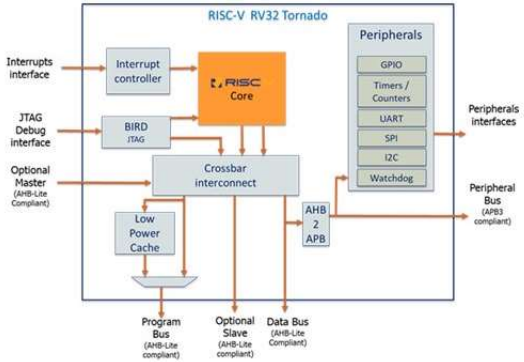
Open-Source is something serious

- RI5CY born to be integrated into PULP
- Verification for an academic Energy-Efficient design group is less important than performance for research purposes
- Open-Source nature of the core attracted companies that verified and evaluated it for us. Reporting bugs and problems on GitHub

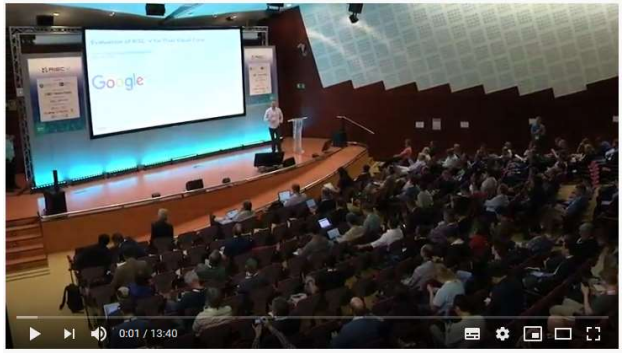
GreenWaves GAP8

NXP Vega board

Dolphin Integration

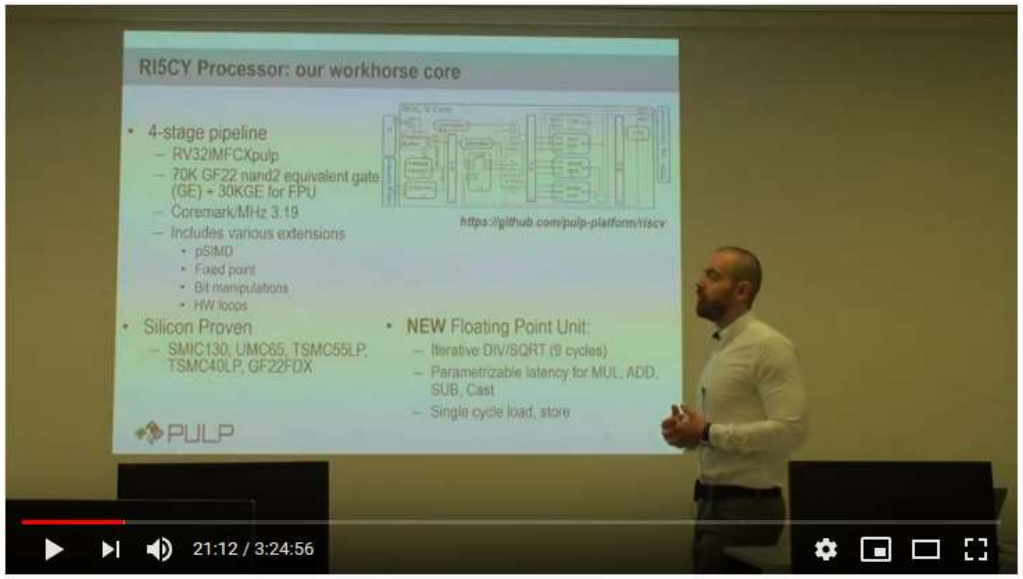


Google and Valtrix



Use of RISC-V on Pixel Visual Core

The PULP training



WOSH: Understanding and working with PULP

- Companies and universities asked for specific « classes »
  - Theory and hands-on
- In home tutorials and Q&A
  - Targetting specif concerns
- Generic tutorial available on youtube
  - (recorded during WOSH Zurich 2019)
  - https://www.youtube.com/watch?v=27tndT6cBH0&t=3429s

The need of industrial support

The graduation day of RI5CY

- The workload to provide support to bug fixes, features requests, questions, documentation is too high for a research group
  - Univerisity does research, not products
- zero-riscy, the little brother of RI5CY moved to LowRISC to be maintained and improved
- June 2019, OpenHW Group announces that RI5CY → **CORE-V CV32E40P** to be verified, improved, and silicon-proven at industrial level

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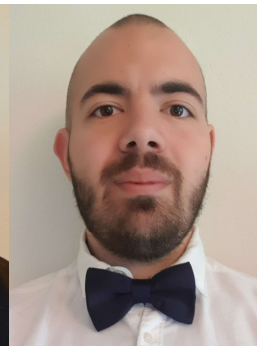
OpenHW Cores Task Group

- CV32E40P is still open-source with the same permissive license
  - But now maintained at industrial quality level
- The Cores Task Group leads the decisions for the CORE-V Family
  - Every member of OpenHW is welcome to discuss with us on mattermost
- Issues, questions, pull requests on GitHub can be done by EVERYONE
  - The Cores Task Group reviews them and decides whether to accept them or not

Chair	Vice-Chair	Director
		
Arjan Bink	Jerome Quevremont	Davide Schiavone

The First Action: Verification as Priority

- CV32E40P is still open-source with the same permissive license
  - But now maintained at the industrial quality level
- Verification is not the focus of a research project and is required for an industry grade product
- OpenHW Group decided based on timeline and resources which features and parameters CV32E40P to implement based on member needs and VERIFICATION effort
  - PULP ISA Extensions kept
  - RISC-V compliant interrupts and performance counters
  - Bug fixes
  - Tandem verification with Imperas ISS
  - Security and Atomics removed, but RTL kept for future versions and forks

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Coding Style Tasks

- CV32E40P changed all the file and module names to be consistent
- Code has been cleaned up and few parameters to make integration easier
- Folders have been re-organized
  - Simulation only vs. real hardware
- The old testbench became a simple example, whereas the verification activity is managed in an ad-hoc repository (core-v-verif)
- Assertions to improve verifications

RISC-V Spec Compliant Tasks

- CV32E40P changed its interrupt scheme with the RISC-V CLINT spec.
- Performance counters now RISC-V compliant
- Bug fixes to make the core compliant

RTL Coding Tasks

- CV32E40P has been updated with a new memory interface AMBA friendly (named Open Bus Interface OBI)
  - Removed combinatorial paths to improve the frequency
  - Can implement multiple out-standing transactions
- New HWLoop logic
- New Instruction Fetch stage

PULP ISA Extentions Tasks

- PULP ISA kept and under verification:
  - CV32E40P masterpiece is a custom ISA developed under the PULP project to make it highly efficient with data-intensive application
- Parametrizable for those who do not need them
  - Core not optimized for this specific case

Documentation Tasks

- RI5CY had word-based documentation
  - Not updated
  - Difficult to maintain
- CV32E40P has been uploaded with text-based documentation
  - Many fixes and updates
  - Based on Sphinx

CV32E40P RTL Freeze one-month from now

- Targetting RTL freeze in October
- Verification the most significant improvement of the core to become industrial level
- The LOOP: Verification team finds bugs in the documentation, RTL, and simulation tracer. Design team fixes them and improve the code.
- Multi OpenHW member company resources assembled in virtual teams to collaborate and create an open-source RISC-V core!

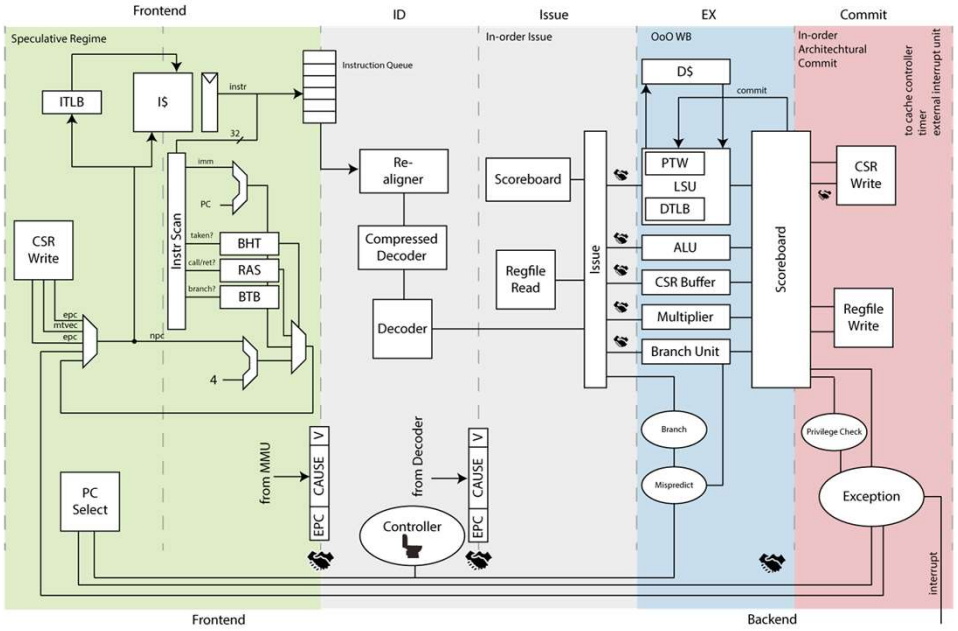
CV3240P Future

- New FPU interface
  - Standard interface based on external accelerator
  - Ideally unblocking pipeline for independent instructions (pseudo dual-issue)
- Adding back user-mode, PMP, and atomics
- Optimizations for FPGA

The need of an application class CPU

- Many applications are based on Operating Systems like Linux
- The PULP team evaluated open-source IPs, but they were based on non-industrial languages back in days
- Ariane is born. A RV64GC core running Linux!

Ariane



- RV64GC
  - RISC-V Debug
- Linux Capable
  - M, S and U privilege modes
  - TLB
  - Tightly integrated D$ and I$
  - Hardware PTW
- 6-stage pipeline
  - In-order issue
  - Out-of-order write-back
  - In-order commit
- Branch-prediction
  - RAS
  - Branch Target Buffer
  - Branch History Table
- Scoreboarding
- 1,5+ GHz in GF22FDX GlobalFoundries

CVA6: the graduation day of Ariane

- As its little brother, Ariane moved to OpenHW
  - Same need for industrial support
- Contribution of members to make it either 64 or 32b → CVA6
  - The name has no bit-width as it is configurable
- New to the family but ready to go on fire!

First top-priority CVA6 tasks

- New documentation
- Build a verification environment to host CVA6
- Review the 32b parameter pull-request
  - Big review effort but a huge benefit
- FPGA optimizations

Call to Action

- CORE-V cores NEED YOU!
  - Become a member of OpenHW Group and help us build the

    FUTURE of OPEN-SOURCE HARDWARE
- Contact us: davide@openhwgroup.org

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Thank you!