Open Source Processor IP
for high-volume production SoCs

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Outline

• Challenges with SoC design and Open Source IP

• OpenHW Group
  • OpenHW Members & Governance
  • CORE-V Family of open source RISC-V cores
  • OpenHW Working Groups & Task Groups

• Summary
SoC Development Cost Drivers

- Software, RTL design, Verification and Physical design account for ~90% of overall SoC development costs.
- For highly differentiated IP blocks and functions, this investment is warranted.
- For general purpose CPU cores an effective open-source model can drive down these development costs and increase re-use across the industry.

Image Source: Arm Ecosystem Blog
Barriers to adoption of Open Source HW IP

• IP quality
  • harness community best-in-class design and verification methods and contributions

• Ecosystem
  • ensure availability of IDE, RTOS / OS ports, physical design etc. and create a roadmap of cores covering a range of PPA metrics

• Permissive use
  • permissive open-source licensing and processes to minimize business and legal risks
RISC-V ISA Brings Open Source Paradigm to CPU Design

• The free and open RISC-V ISA unleashes a new frontier of processor design and innovation

• How many open source processor implementations do we need as an industry?
  • Open cores are great from a pedagogical teaching perspective, but how many is too many for widespread industry adoption?

• How does the industry, ecosystem, community organize to ensure open core success?
  • How do we establish critical mass around a handful of open cores?
# Many RISC-V Open Source Cores...

...and counting....

(source: riscv.org)

<table>
<thead>
<tr>
<th>Name</th>
<th>Maintainer</th>
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• **OpenHW Group** is a not-for-profit, global organization driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the **CORE-V** Family of open-source RISC-V cores

• International footprint with developers in North America, Europe and Asia
• Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices
• Strong support from industry, academia and individual contributors with 53+ members and partners worldwide
Partner Ecosystem
53+ Members & Partners

Legal, Accounting, Banking

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• Rick O’Connor, OpenHW Group (non-voting)
Working Groups & Task Groups

• Board appoints Chairs of ad-hoc working groups and has final approval of working group recommendations
  • Technical Working Group and Marketing Working Group will be standing working groups

• Technical Working Group
  • Cores Task Group
  • Verification Task Group
  • SW Task Group
  • HW Task Group

• Marketing Working Group
  • University Outreach Task Group

• Together with internal OpenHW Group engineering staff, member company development engineers (FTEs / ACs) establish and execute OpenHW Group projects
Technical Working Group (TWG)

• Co-Chairs
  • Sebastian Ahmed, Silicon Laboratories
  • Jerry Zeng, NXP Semiconductors

• Drive the overall technical direction, development roadmap and project execution for all technology related activities within the OpenHW Group and oversee the Task Groups
  • TWG is essentially the OpenHW Group company’s “R&D / Engineering Organization”

• OpenHW Group engineering release methodology is based on the Eclipse Development Process
  • All OpenHW Group Platinum / Gold / Silver members are also Solutions members of the Eclipse Foundation
Cores Task Group

- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology
- develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.
- Initial contribution of open source RISC-V cores from ETH Zurich PULP Platform and the OpenHW Group is the official committer for these repositories

<table>
<thead>
<tr>
<th>Core</th>
<th>Bits/Stages</th>
<th>Description</th>
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<tbody>
<tr>
<td>CVE4 (RISCY)</td>
<td>32bit / 4-stage</td>
<td>A 4-stage core that implements, the RV32IMFCXpulp, has an optional 32-bit FPU supporting the F extension and instruction set extensions for DSP operations, including hardware loops, SIMD extensions, bit manipulation and post-increment instructions.</td>
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<tr>
<td>CVA6 (Ariane)</td>
<td>32 &amp; 64bit / 6-stage</td>
<td>A 6-stage, single issue, in-order CPU implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. It has configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).</td>
</tr>
</tbody>
</table>
Verification Task Group

• Co-Chairs:
  • Leo Wang, Futurewei Technologies, Inc.
  • Steve Richmond, Silicon Laboratories

• develop best in class verification test bench environments for the cores and IP blocks developed within the OpenHW Group.
CORE-V Verification Test Bench
UVM Environment

- Manually written Test-Programs
- Random Instruction Generator
- Most test-programs from Google generator
- Instruction Memory loaded from hexfile
- Memory Mapped Virtual Peripherals
- Toolchain invoked by UVM run-flow
- GCC compile elf2hex
crt0.S link.ld
Test-Program Environment

Speech recognition from Manual written Test-Programs

- Instruction Memory
- Memory Mapped Virtual Peripherals
- Random Instruction Generator
- Most test-programs from Google generator
- Toolchain invoked by UVM run-flow
- GCC compile elf2hex
crt0.S link.ld
Test-Program Environment

- Make SIMULATOR=<sim> +UVM_TEST=riscv-dv-test
- UVM RISC-V Reference Model
- RM runs same program as Core
- Agents driven by UVM Sequences independent of Test-Program
- Interrupt Agent
- Debug Agent
- All CSRs, GPRs & PC
- Step & Compare
- Re-use Assertions from Formal Verification

Functional Coverage

SVA

GCC
compile
elf2hex
crt0.S
link.ld
Test-Program Environment

Random Instruction Generator

Most test-programs from Google generator

Toolchain invoked by UVM run-flow

GCC compile elf2hex
crt0.S link.ld
Test-Program Environment

make SIMULATOR=<sim> +UVM_TEST=riscv-dv-test

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SW Task Group

• Chair: Jeremy Bennett, Embecosm
• Vice-Chair: Yunhai Shang, Alibaba T-Head

• define, develop and support SW tool chain, operating system ports and firmware for the cores and IP developed within the OpenHW Group.
HW Task Group

• Chair: Hugh Pollitt-Smith, CMC Microsystems
• Vice-Chair: Tim Saxe, QuickLogic
• define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group.
• Initial project using Digilent Genesys2 FPGA boards for soft-core bring up for both CV32E4 and CV64A6
What’s Next? Some Predictions...

1. OpenHW Group ecosystem will continue to grow
   • 53 Members & Partners now – expect over 60 by end of 2020

2. New open source RISC-V cores added to the CORE-V Family
   • CV32E4 and CV64A6 now – CV32E0, CV32A6 and more to come

3. On chip SoC interconnect (fabric & busses)

4. Heterogeneous clusters leveraging eFPGA
• OpenHW Group established to create a viable open source ecosystem for the semiconductor industry
  • OpenHW Group is a not-for-profit corporation
  • International footprint with developers in North America, Europe and Asia
  • Strong support from industry, academia and individual contributors

• OpenHW Group & CORE-V Family of open-source RISC-V cores
  • Proven System Verilog CV64A6 and CV32E4 core designs, processor sub-system IP blocks, verification test bench, and reference designs
  • Visit www.openhwgroup.org for further details

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