Open Source Processor IP

for high-volume production SoCs

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Outline

- Challenges with SoC design and Open Source IP

- OpenHW Group
  - OpenHW Members & Governance
  - CORE-V Family of open source RISC-V cores
  - OpenHW Working Groups & Task Groups

- Summary

SoC Development Cost Drivers

- Software, RTL design, Verification and Physical design account for ~90% of overall SoC development costs
- For highly differentiated IP blocks and functions, this investment is warranted
- For general purpose CPU cores an effective open-source model can drive down these development costs and increase re-use across the industry

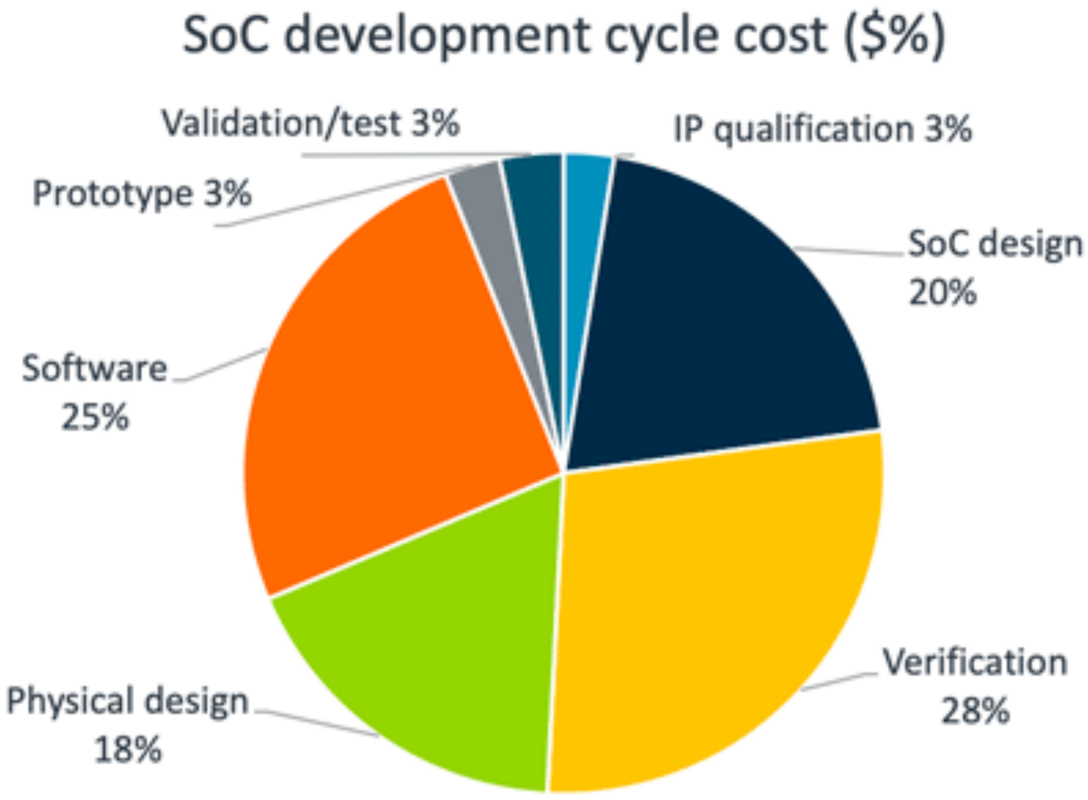


Image Source: Arm Ecosystem Blog

Barriers to adoption of Open Source HW IP

- IP quality
  - harness community best-in-class design and verification methods and contributions
- Ecosystem
  - ensure availability of IDE, RTOS / OS ports, physical design etc. and create a roadmap of cores covering a range of PPA metrics
- Permissive use
  - permissive open-source licensing and processes to minimize business and legal risks

RISC-V ISA Brings Open Source Paradigm to CPU Design

- The free and open RISC-V ISA unleashes a new frontier of processor design and innovation
- How many open source processor implementations do we need as an industry?
  - Open cores are great from a pedagogical teaching perspective, but how many is too many for widespread industry adoption?
- How does the industry, ecosystem, community organize to ensure open core success?
  - How do we establish critical mass around a handful of open cores?

Many RISC-V Open Source Cores… …and counting….

(source: riscv.org)

Name	Maintainer	Links	User spec	License
rocket	SiFive, UCB Bar	GitHub	2.3-draft	BSD
freedom	SiFive	GitHub	2.3-draft	BSD
Berkeley Out-of-Order Machine (BOOM)	Esperanto, UCB Bar	GitHub	2.3-draft	BSD
ORCA	VectorBlox	GitHub	RV32IM	BSD
RI5CY	ETH Zurich, Università di Bologna	GitHub	RV32IMC	Solderpad Hardware License v. 0.51
Zero-riscy	ETH Zurich, Università di Bologna	GitHub	RV32IMC	Solderpad Hardware License v. 0.51
Ariane	ETH Zurich, Università di Bologna	Website,GitHub	RV64GC	Solderpad Hardware License v. 0.51
Riscy Processors	MIT CSAIL CSG	Website,GitHub		MIT
RiscyOO	MIT CSAIL CSG	GitHub	RV64IMAFD	MIT
Lizard	Cornell CSL BRG	GitHub	RV64IM	BSD

Name	Maintainer	Links	User spec	License
Minerva	LambdaConcept	GitHub	RV32I	BSD
OPenV/mriscv	OnChipUIS	GitHub	RV32I(?)	MIT
VexRiscv	SpinalHDL	GitHub	RV32I[M][C]	MIT
Roa Logic RV12	Roa Logic	GitHub	2.1	Non-Commercial License
SCR1	Syntacore	GitHub	2.2, RV32I/E[MC]	Solderpad Hardware License v. 0.51
Hummingbird E200	Bob Hu	GitHub	2.2, RV32IMAC	Apache 2.0
Shakti	IIT Madras	Website,GitLab	2.2, RV64IMAFDC	BSD
ReonV	Lucas Castro	GitHub		GPL v3
PicoRV32	Clifford Wolf	GitHub	RV32I/E[MC]	ISC
MR1	Tom Verbeure	GitHub	RV32I	Unlicense
SERV	Olof Kindgren	GitHub	RV32I	ISC
SweRV EH1	Western Digital Corporation	GitHub	RV32IMC	Apache 2.0
Reve-R	Gavin Stark	GitHub	RV32IMAC	Apache 2.0

OpenHW and CORE-V

- OpenHW Group is a not-for-profit, global organization driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the CORE-V Family of open-source RISC-V cores
  - International footprint with developers in North America, Europe and Asia
  - Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices
  - Strong support from industry, academia and individual contributors with 53+ members and partners worldwide

Industry Ecosystem
53+ Members & Partners

OPENHW GROUP™ — PROVEN PROCESSOR IP

CORE-V™

Alibaba Group 阿里巴巴集团

bluespec

BSC Barcelona Supercomputing Center
Centro Nacional de Supercomputación

FUTUREWEI Technologies

NXP

SILICON LABS

VeriSilicon

AB Open

ASHLING

axiomise — predictable formal verification

beagleboard.org

BTA DESIGN SERVICES — your project, our team

DATUM

ECSPEC

em microelectronic

EMBECOSM®

GF®

GREENWAVES TECHNOLOGIES

HENSOLDT — Detect and Protect.

HUAWEI

IAR SYSTEMS

imperas

inzone.ai

metrics

NVIDIA.

onespin

> OPERSYS

PRAESUM COMMUNICATIONS

QuickLogic®

SECURE THINGZ

Symbiotic EDA

THALES

ultraSoC

Research Ecosystem

53+ Members & Partners

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

CMC MICROSYSTEMS

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

ETH zürich

ÉTS Le génie pour l'industrie
ÉCOLE DE TECHNOLOGIE SUPÉRIEURE
Université du Québec

Mitacs

POLYTECHNIQUE MONTRÉAL
WORLD-CLASS ENGINEERING

uOttawa

UNIVERSITY OF TORONTO

THE UNIVERSITY OF UTAH®

Partner Ecosystem

53+ Members & Partners

Legal, Accounting, Banking

OpenHW Group Board of Directors

- Rob Oshana, NXP (Chairman)
- Charlie Hauck, Bluespec (Treasurer)
- Xiaoning Qi, Alibaba Group
- John Davis, Barcelona Supercomputing Center
- Liang Peng, Futurewei Technologies
- Alessandro Piovaccari, Silicon Labs
- Wayne Dai, VeriSilicon
- Rick O'Connor, OpenHW Group (non-voting)

Working Groups & Task Groups

- Board appoints Chairs of ad-hoc working groups and has final approval of working group recommendations
  - Technical Working Group and Marketing Working Group will be standing working groups
- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - SW Task Group
  - HW Task Group
- Marketing Working Group
  - University Outreach Task Group
- Together with internal OpenHW Group engineering staff, member company development engineers (FTEs / ACs) establish and execute OpenHW Group projects

Technical Working Group (TWG)

- Co-Chairs
  - Sebastian Ahmed, Silicon Laboratories
  - Jerry Zeng, NXP Semiconductors
- Drive the overall technical direction, development roadmap and project execution for all technology related activities within the OpenHW Group and oversee the Task Groups
  - TWG is essentially the OpenHW Group company's "R&D / Engineering Organization"
- OpenHW Group engineering release methodology is based on the Eclipse Development Process
  - All OpenHW Group Platinum / Gold / Silver members are also Solutions members of the Eclipse Foundation

Cores Task Group

- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology
- develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.
- Initial contribution of open source RISC-V cores from ETH Zurich PULP Platform and the OpenHW Group is the official committer for these repositories

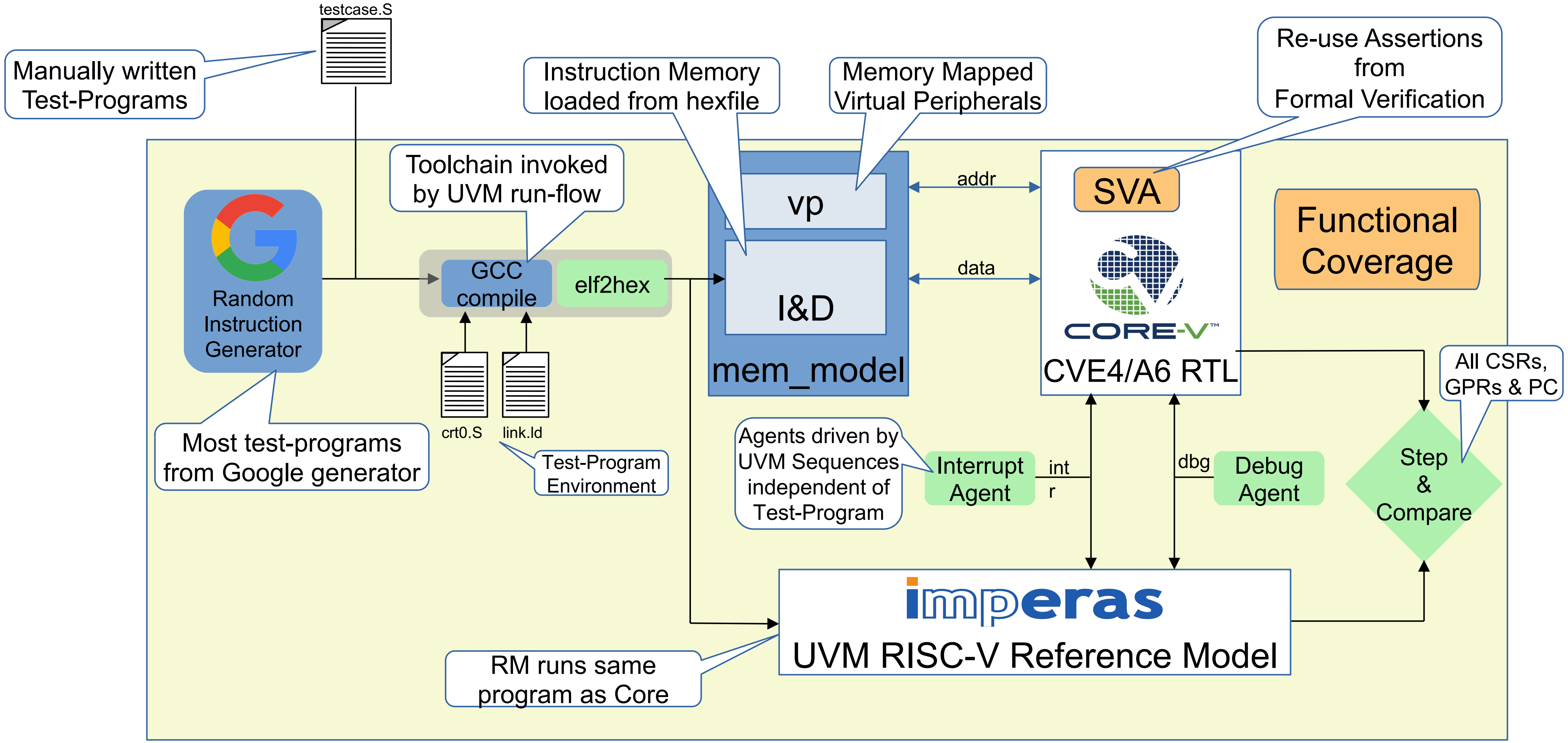
Core	Bits/Stages	Description
CVE4 (RI5CY)	32bit / 4-stage	A 4-stage core that implements, the RV32IMFCXpulp, has an optional 32-bit FPU supporting the F extension and instruction set extensions for DSP operations, including hardware loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	32 & 64bit / 6-stage	A 6-stage, single issue, in-order CPU implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. It has configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

Verification Task Group

- Co-Chairs:
  - Leo Wang, Futurewei Technologies, Inc.
  - Steve Richmond, Silicon Laboratories

- develop best in class verification test bench environments for the cores and IP blocks developed within the OpenHW Group.

CORE-V Verification Test Bench
UVM Environment



make SIMULATOR=<sim> +UVM_TEST=riscv-dv-test

SW Task Group

- Chair: Jeremy Bennett, Embecosm
- Vice-Chair: Yunhai Shang, Alibaba T-Head

- define, develop and support SW tool chain, operating system ports and firmware for the cores and IP developed within the OpenHW Group.

HW Task Group

- Chair: Hugh Pollitt-Smith, CMC Microsystems
- Vice-Chair: Tim Saxe, QuickLogic
- define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group.
- Initial project using Digilent Genesys2 FPGA boards for soft-core bring up for both CV32E4 and CV64A6

What's Next? Some Predictions…

1. OpenHW Group ecosystem will continue to grow
   - 53 Members & Partners now – expect over 60 by end of 2020

2. New open source RISC-V cores added to the CORE-V Family
   - CV32E4 and CV64A6 now – CV32E0, CV32A6 and more to come

3. On chip SoC interconnect (fabric & busses)

4. Heterogeneous clusters leveraging eFPGA

OPENHW GROUP and CORE-V

- OpenHW Group established to create a viable open source ecosystem for the semiconductor industry
  - OpenHW Group is a not-for-profit corporation
  - International footprint with developers in North America, Europe and Asia
  - Strong support from industry, academia and individual contributors
- OpenHW Group & CORE-V Family of open-source RISC-V cores
  - Proven System Verilog CV64A6 and CV32E4 core designs, processor sub-system IP blocks, verification test bench, and reference designs
  - Visit www.openhwgroup.org for further details
- Follow us on Social media
  - Twitter @openhwgroup and LinkedIn OpenHW Group