Learn - Adopt - Produce

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OPEN SOURCE DEVELOPER FORUM

CORE-V™ Family of RISC-V Cores

- Initial contribution of open source RISC-V cores from ETH Zurich PULP Platform
  - Very popular, industry adopted cores
- OpenHW Group becomes the official committer for these repositories

ETH zürich PULP Parallel Ultra Low Power

CORE-V™ RISC-V®

Core	Bits/Stages	Description
CVE4 (RI5CY)	Embedded 32 bit 4-stage	An Embedded class 4-stage core that implements, the RV32IMFCXpulp, has an optional 32-bit FPU supporting the F extension and instruction set extensions for DSP operations, including hardware loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	Application 32 & 64 bit 6-stage	An Application class 6-stage, single issue, in-order CPU implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. It has configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

CORE-V™ MCU SoC
Tapeout Early Q1 2021

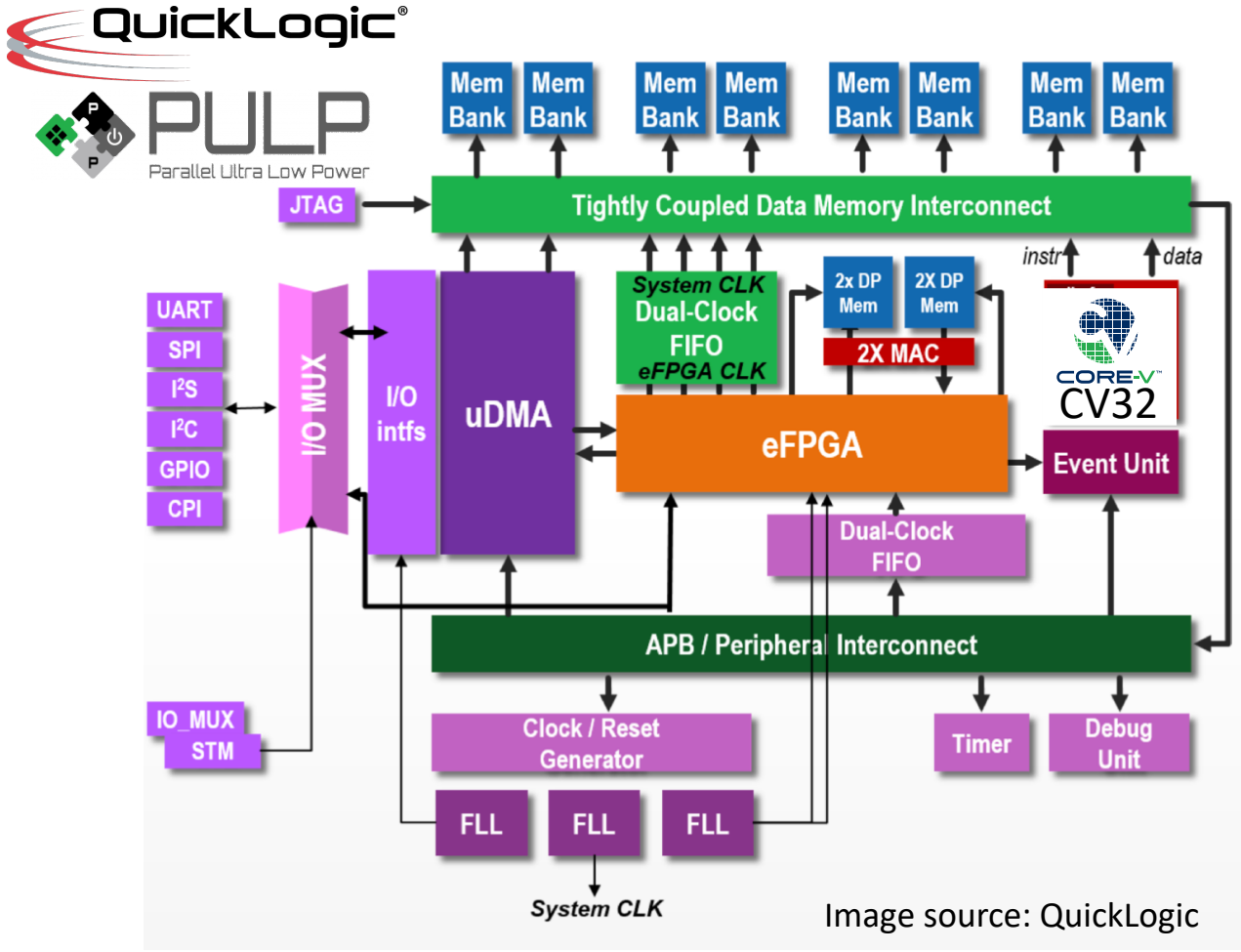


Image source: QuickLogic

- Project announced at Open Source Developer Forum Sept 2020
- Real Time Operating System (e.g. Zephyr) capable ~600+MHz CV32 MCU host CPU
- Embedded FPGA fabric with hardware accelerators from QuickLogic
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX

You are welcome to participate!

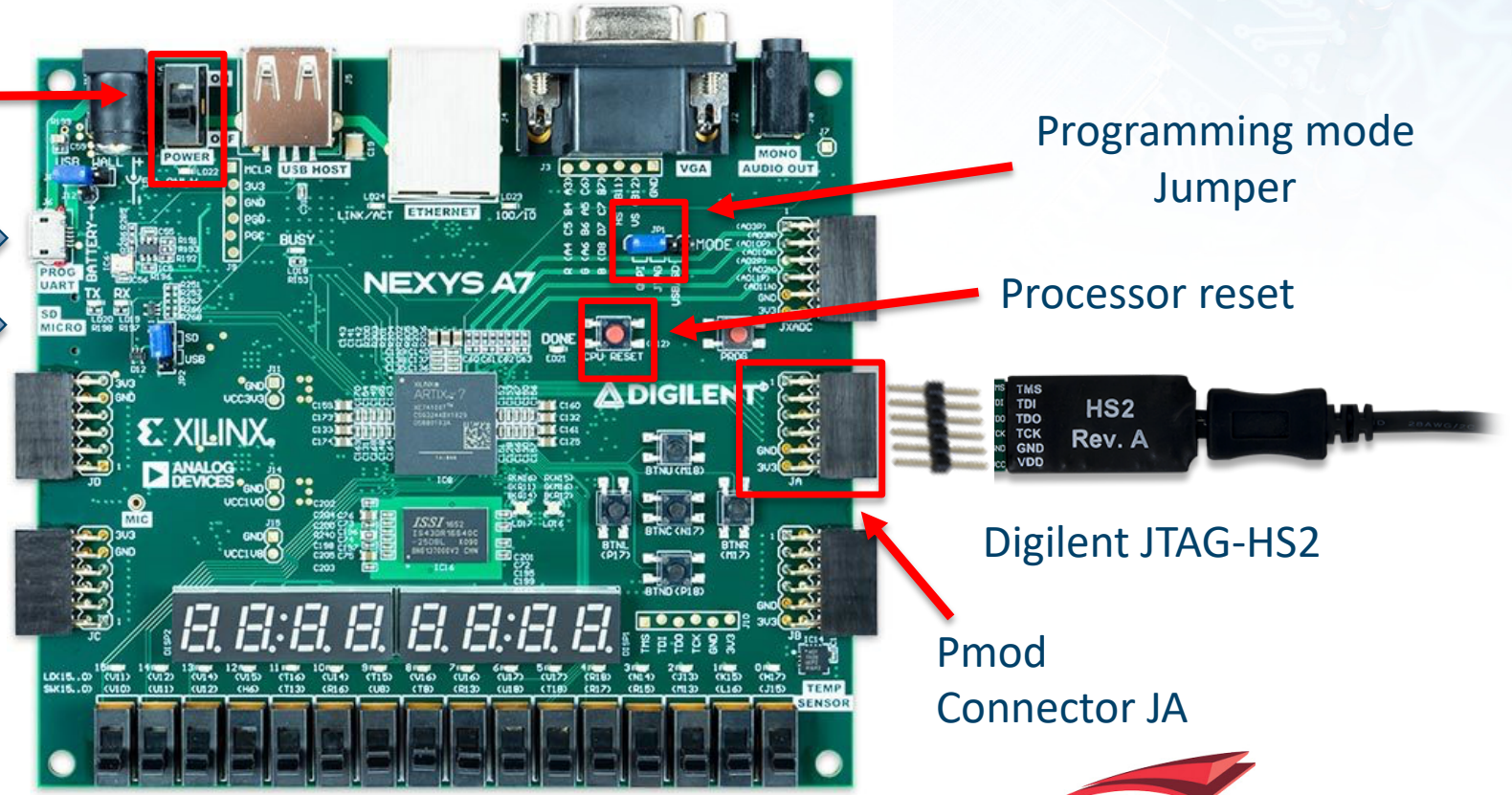
1. Create account at https://www.eclipse.org/
2. Sign Eclipse Contributor Agreement (electronically)
3. Specify your GitHub id in your Eclipse profile
4. Fork https://github.com/openhwgroup/core-v-ide-cdt
5. Don’t forget to add “signed-off-by” to commit message

Example:

```
Signed-off-by: Alexander Fedorov <alexander.fedorov@arsysop.ru>
```

ECLIPSE FOUNDATION

Digilent NexysA7-100T FPGA Board



CORE-V™ MCU FPGA

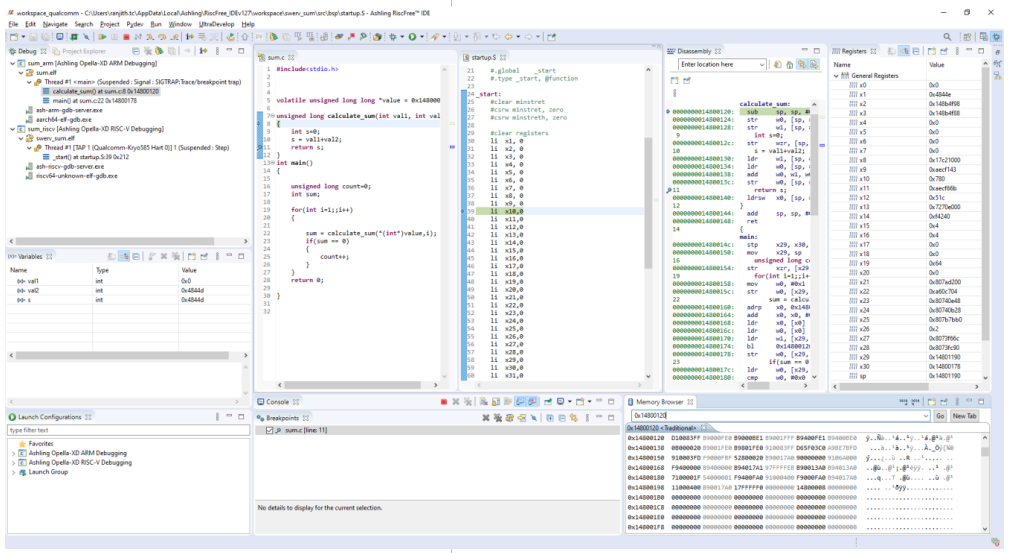
CORE-V™ GCC Tools – Get Involved!

- As a user
  - download the latest development tool chains
  - embecosm.com/resources/tool-chain-downloads
  - pre-built binaries, source code, scripts and test results
- As a developer
  - join the OpenHW Mattermost SW : GNU Tools channel
  - sign up the OpenHW SW mailing list and attend the monthly meeting
  - submit your pull requests against the **`development`** branch
    - github.com/openhwgroup/corev-binutils-gdb
    - github.com/openhwgroup/corev-gcc

EMBECOSM®

CORE-V IDE

- ***CORE-V IDE*** is a freely available, open-source development environment created by the OpenHW group
- Eclipse based IDE for CORE-V development
- Includes the Compiler Toolchain for CORE-V provided by Embecosm
- OpenOCD Debug Support
- “Ready-to-run” examples for Digilent boards
- Getting started guide
- Available end September 2020



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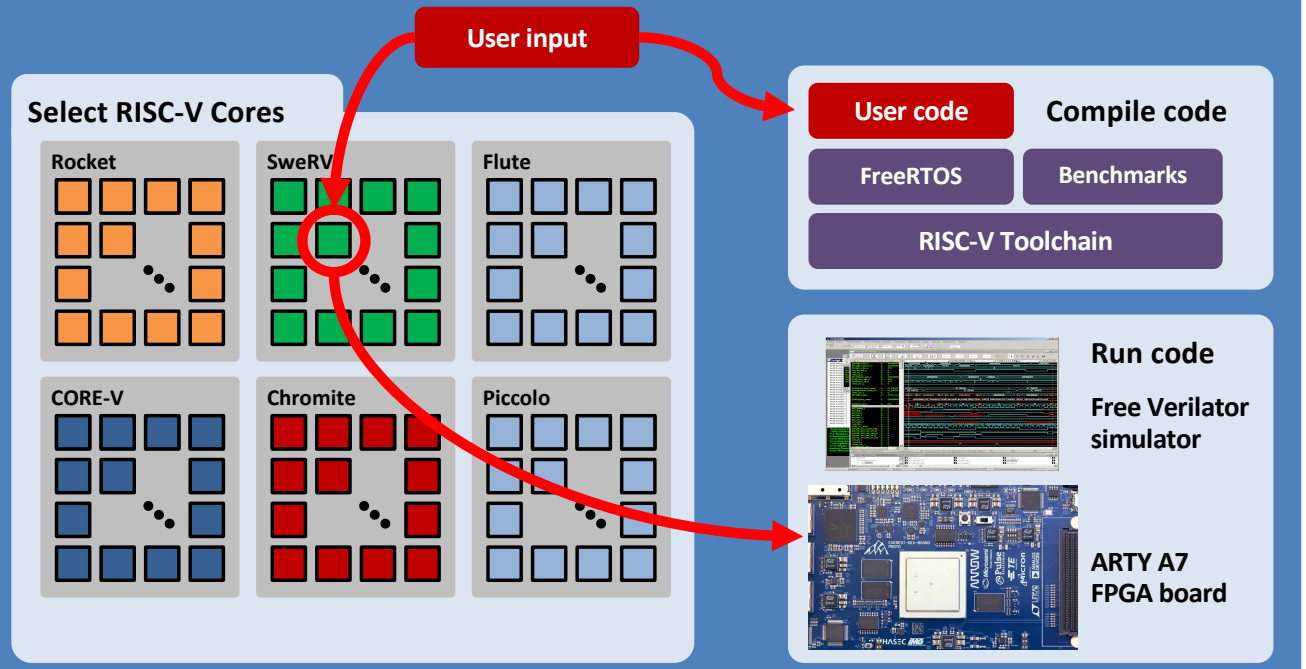
RISC-V *Explorer* – Bluespec's free RISC-V core evaluation tool

Select from hundreds of pre-built and pre-tested RISC-V cores.

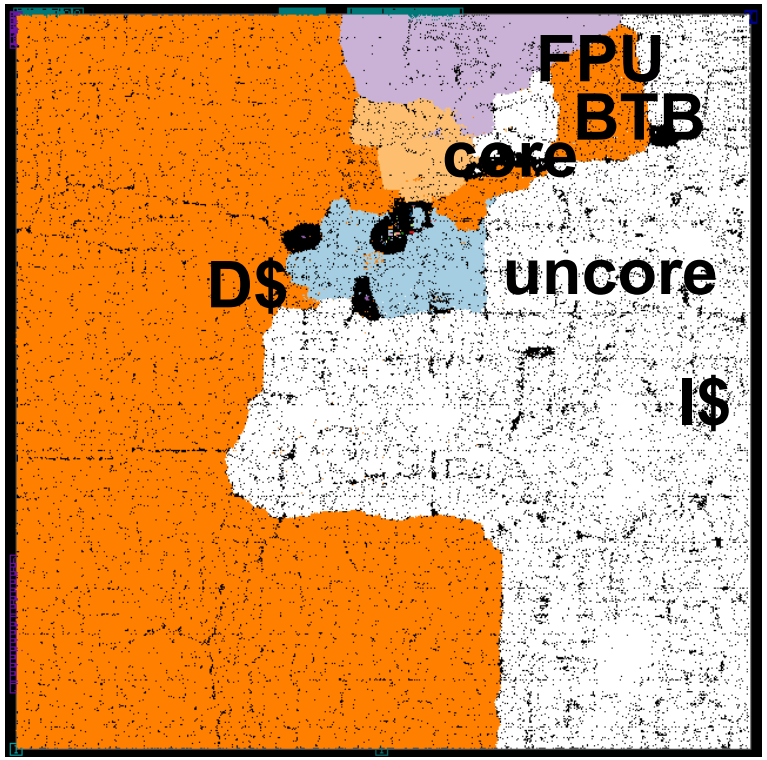
Compile and **run** your application code with zero setup time or effort.

Connect to low cost FPGA board for high-speed execution and debug.



RISC-V So Far

- RV64G ISA
  - 64-bit
  - integer multiplication and division
  - single & double precision FP
- Open source Rocket
  - from Chipyard
    - Berkeley Arch. Research
  - from Bespoke Silicon Group
  - I$ 4 KiB; D$ 4 KiB
    - 64 set, 4-way
- Technology
  - FD-SOI GF 22-nm
  - SSS (0.72 V) → 500 MHz
  - FFF (0.88 V) → 950 MHz



Rocket

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2021 – Save the Date!

- Expanded 2 day event
- Tuesday & Wednesday September 14-15, 2021
- Ottawa, ON Canada