CORE-V CVE4 in Bluespec RISC-V Explorer

Tuesday September 15

4:15pm EDT

Bluespec provides verified, supported RISC-V open source cores

GitHub repositories

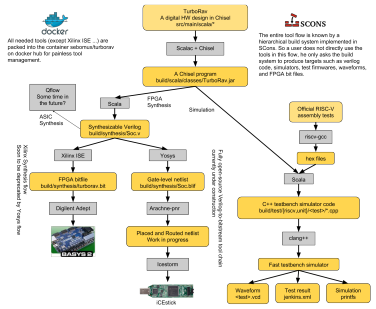
UCB/SiFive

WDC/CHIPS Alliance

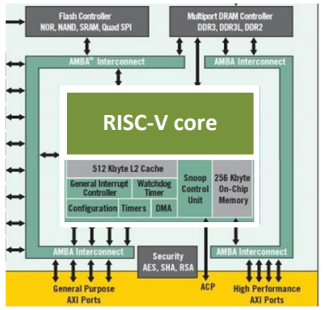
OpenHW

Bluespec

Best-in-Class
RISC-V open source cores
⇩
proprietary quality +
open source benefits



Configure & Generate



Integrate HW & SW

Bluespec, Inc.

Verify & Validate

Bluespec Silicon IP package

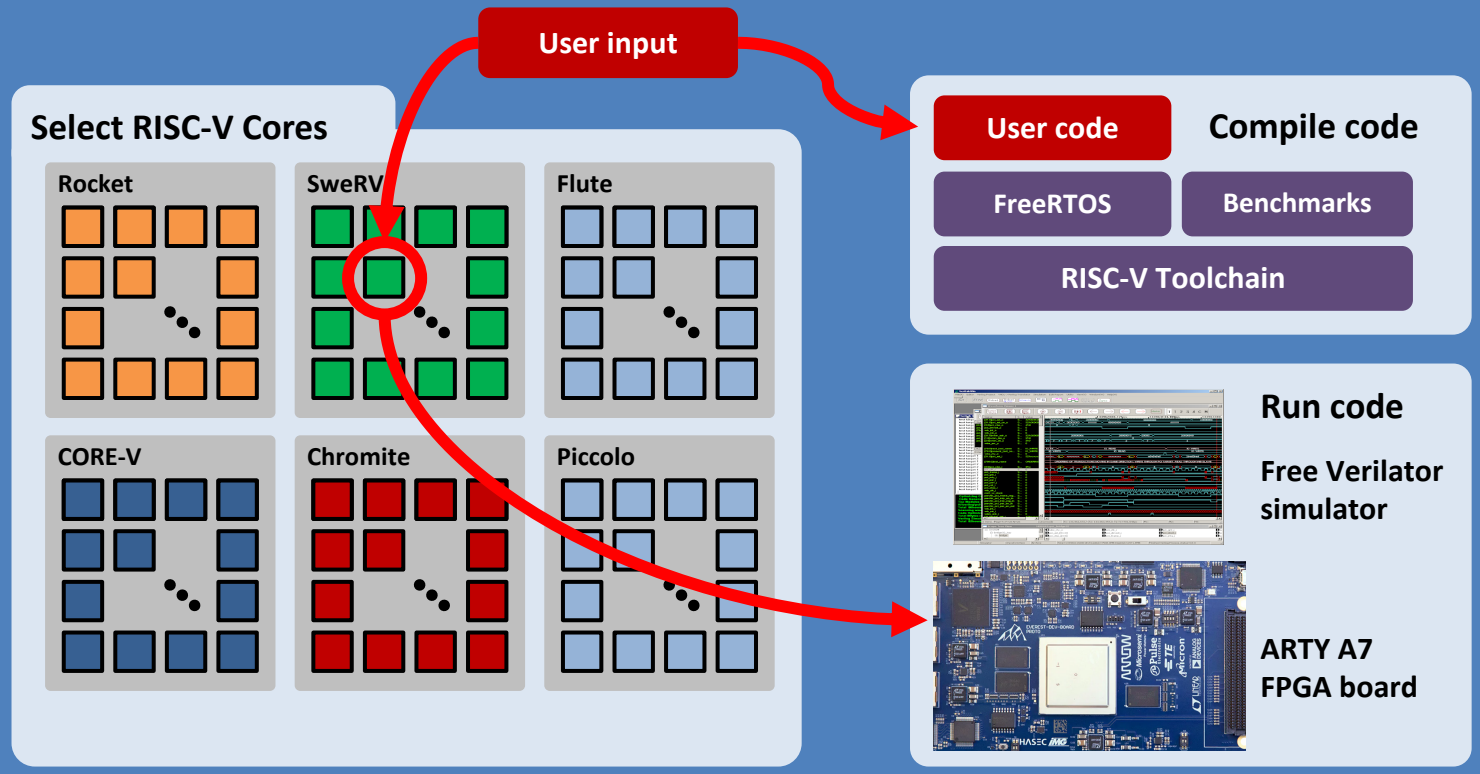
- Synthesizable Verilog
- Verification report
- Reference designs
- Reference software
- Tool chain integration

RISC-V *Explorer* – Bluespec's free RISC-V core evaluation tool

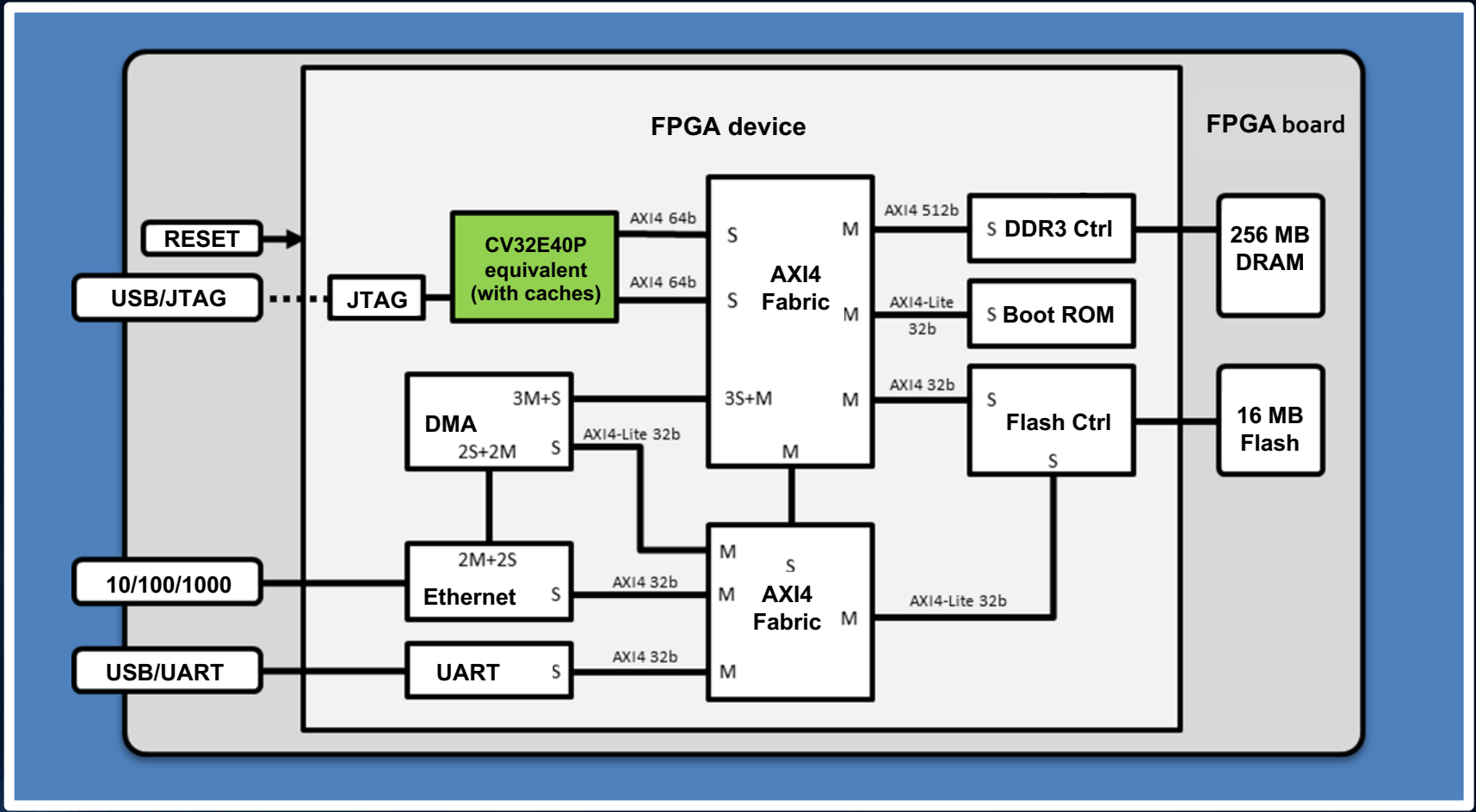
Select from hundreds of pre-built and pre-tested RISC-V cores.

Compile and **run** your application code with zero setup time or effort.

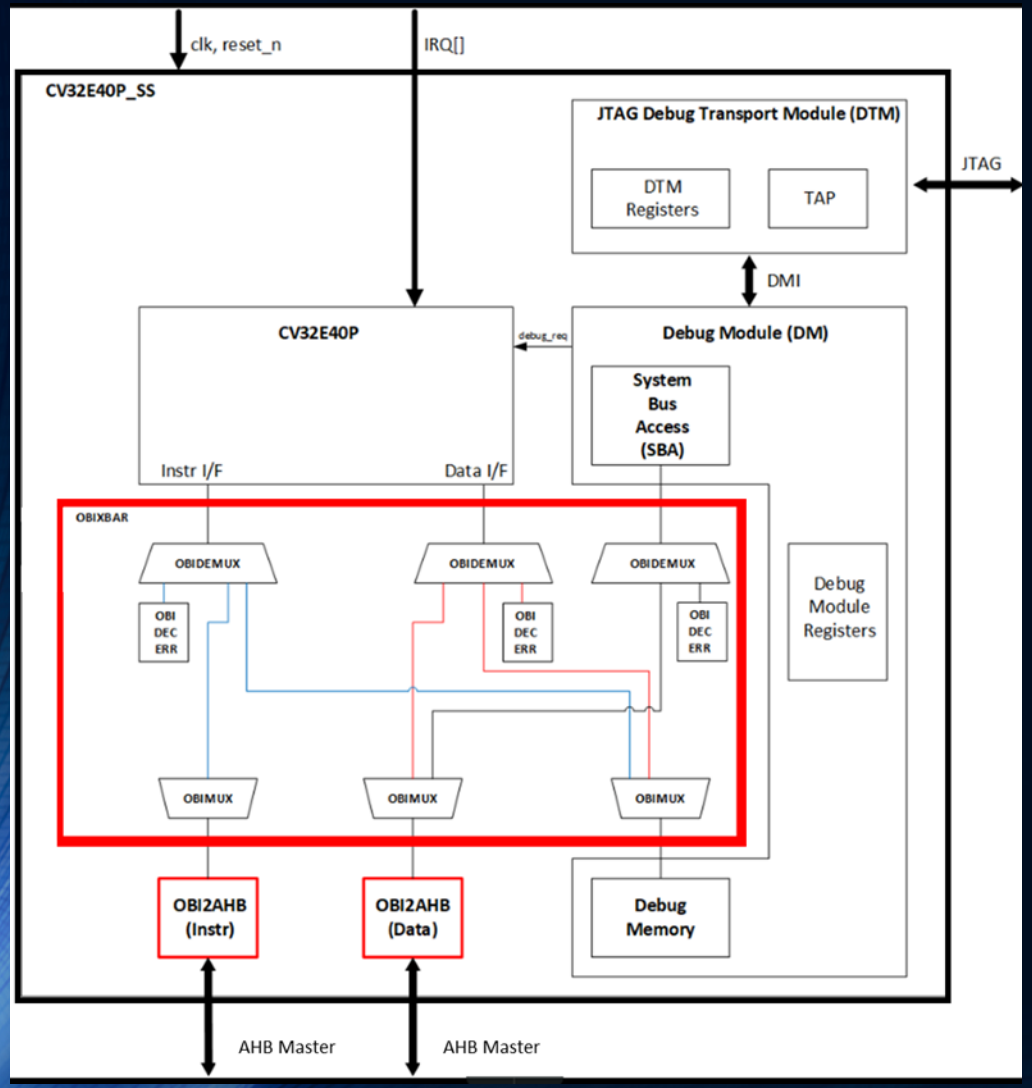
Connect to low cost FPGA board for high-speed execution and debug.

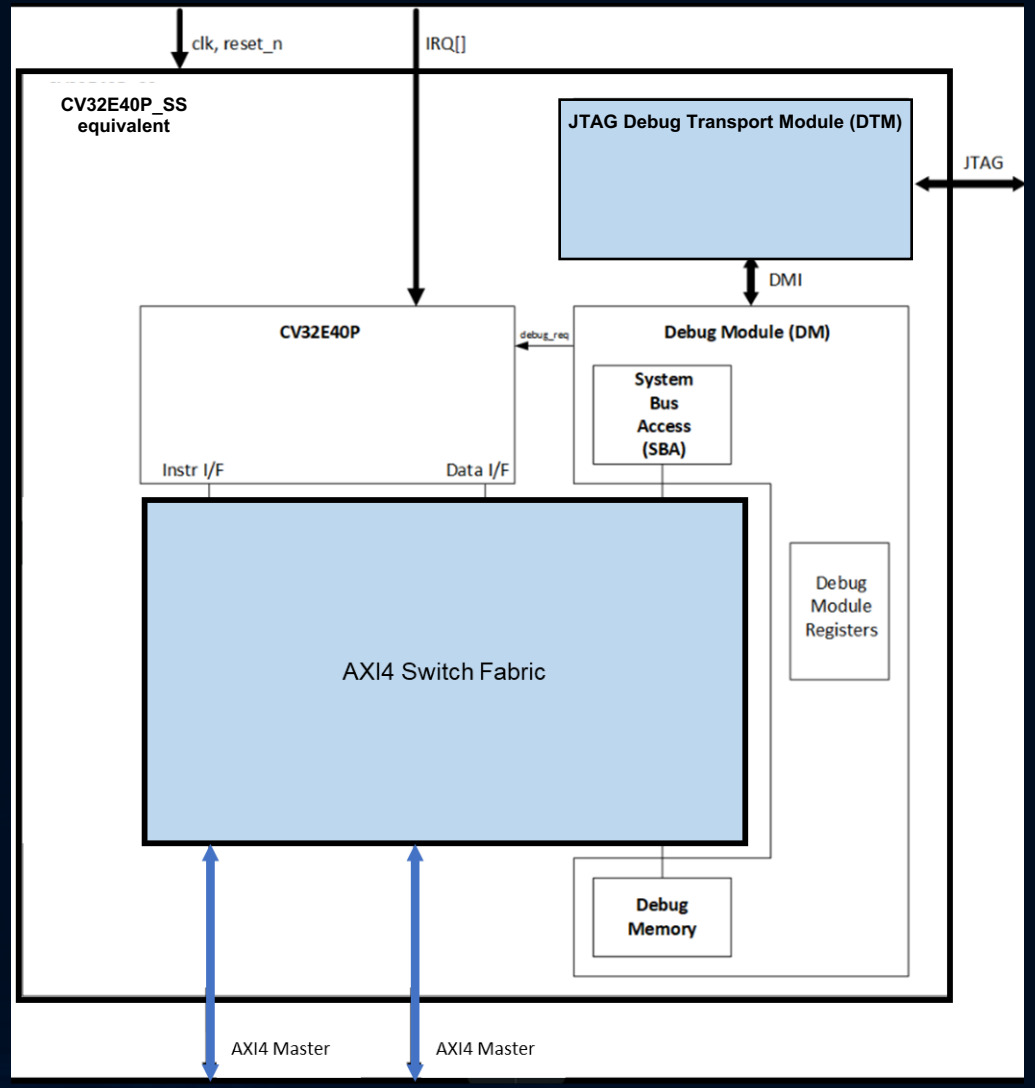


Arty A7 Board with *Explorer* SoC



Integrating the CV32E40P_SS into the RISC-V *Explorer*





Comparison to Piccolo, Flute and Rocket cores

Architecture	CV32E40P	Piccolo	Flute	Rocket
ISA	RV32IMC	RV32IMAC	RV32IMAC	RV32IMAC
Pipeline stages	4	3	5	5
CoreMark	2.23	2.64	2.52	3.21

45nm (CPU pipeline)

Gates	NA*	129K	117K	138K
Frequency		202 MHz	327 MHz	326 MHz

Ultrascale+ (CPU pipeline)

LUTs	5,148	4,223	4,015	5,349
Frequency	111 MHz	71 MHz	142 MHz	250 MHz

*Yosys does not support full SystemVerilog language

Arty A7 Demos

Demo	Processor	Caches*	Program	Comment
1	CV32E40P	4KB	RISC-V ISA tests	It's functional!
2			FreeRTOS blinky	
3	CV32E40P	4KB	"LED color"	Color changes indicate micro-architectural performance
4	Piccolo			
5	Piccolo	4KB	CoreMark	2.23 versus 2.64 confirms the color test!
6	CV32E40P			

*CV32E40P without caches – i.e. straight to DRAM through the fabric – is 20 to 30 times slower.

Thank You

Charlie Hauck
Joe Stoy