Using the CORE-V MCU FPGA Platform

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Agenda

- About CMC Microsystems
- Architecture of the CORE-V MCU FPGA Platform
- CORE-V MCU FPGA Platform Development Environment
- CORE-V MCU FPGA Platform setup
- Demo: Building and Running an Application
- Next steps
Canada’s National Design Network®

A Canada-wide collaboration between 67 universities/colleges to connect 10,000 academic participants with 1,000 companies to design, make and test micro-nanosystem prototypes.

2019-20 Outcomes
3 460 publications
170 awards
85 patents awarded
450 collaborations with industry
10 new startups
625 trained HQP moved to industry

Annually
1 275 connected professors
8 350 researchers
6 575 users of computer aided design tools
200 physical prototypes
75 equipment rental items otherwise unaffordable to users
Lowering barriers to technology adoption

**CAD**
- State-of-the-art environments for successful design
  - Selection of high-performance Computer Aided Design (CAD) tools and design environments
  - Available via desktop or through CMC Cloud
  - User guides, application notes, training materials and courses

**FAB**
- Services for making working prototypes
  - Multi-project wafer services with affordable access to foundries worldwide
  - Fabrication and travel assistance to prototype at a university-based lab
  - Value-added packaging and assembly services
  - In-house expertise for first-time-right prototypes

**LAB**
- Device validation to system demonstration
  - Access to platform-based microsystems design and prototyping environments
  - Access to test equipment on loan
  - Access to contract engineering services

Contact: info@cmc.ca
Architecture of the CORE-V MCU FPGA
PULPissimo/CORE-V MCU
core-v-mcu repo directories

- doc
- fpga
  - README.md
  - cv32e40p_bitstreams
  - cv32e40p_modified_files
  - pulpissimo
    - pulpissimo_nexys
- ips
- rtl
- sim
core-v-mcu/ips/

- adv_dbg_if
- apb
- apb_interrupt_cntrl
- axi
- common_cells
- cv32e40p
- fpnew
- fpu_div_sqrt_mvp
- generic_FLL
- hwpe_ctrl
- hwpe_mac_engine
- hwpe-stream
- jtag_pulp
- L2_tcdm_hybrid_interco
- pulp_soc
- riscv -> cv32e40p
- riscv_dbg
- scm
- tbtools
- tech_cells_generic
- timer_unit
- udma
Documentation

CV32E40P:


PULPissimo/CORE-V MCU:

core-v-mcu FPGA Development Environment
Design Environment

- Ubuntu 18.04
- Xilinx Vivado (2019.2) – WebPack is sufficient for NexysA7
- Mentor Graphics Questasim
- CORE-V GCC toolchain
- PULP-runtime
- PULP-SDK
  - OpenOCD
CORE-V MCU FPGA Platform Setup
Digilent NexysA7-100T FPGA Board

- Power ON/OFF
- Shared UART/JTAG
- MicroSD
- Programming mode Jumper
- Processor reset
- Digilent JTAG-HS2
- Pmod Connector JA

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Demo: Running an application

https://github.com/openhwgroup/core-v-mcu/blob/master/fpga/cv32e40p_modified_files/cv32e40p_sort.tar.gz
CORE-V MCU project
https://github.com/openhwgroup/core-v-mcu/

fpga subfolder contains detailed instructions to:

• Install the CORE-V MCU environment

• Install and modify PULPissimo to instantiate CV32E40P and build the FPGA bitstream

• Download a pre-built FPGA bitstream

• Build and run an application on CV32E40P
Next steps
Get involved, contribute

- Use the platform, provide feedback, raise issues
- Enhance the architecture
- Integrate board peripherals, develop device drivers
- Demonstrate new tools (HW, SW, OS) in the environment
- Develop the runtime, SDK
- Develop applications and demos