

CORE-V IDE

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Agenda

- About Ashling
- Integrated Development Environments
 - CORE-V IDE
 - RiscFree IDE
- CORE-V Demo
 - How to build and debug a CORE-V example program within the IDE

Ashling Introduction

- Development tools for embedded processors and MCUs
- IDEs, Compilers, Debuggers, Hardware Debug and Trace Probes for a range of embedded architectures
- Engineering services for custom tools requirements
- Expertise in complex real-time debug tools including
 - high speed debug connections
 - high capacity real-time trace probes
 - code coverage analysis, profiling, performance analysis etc.

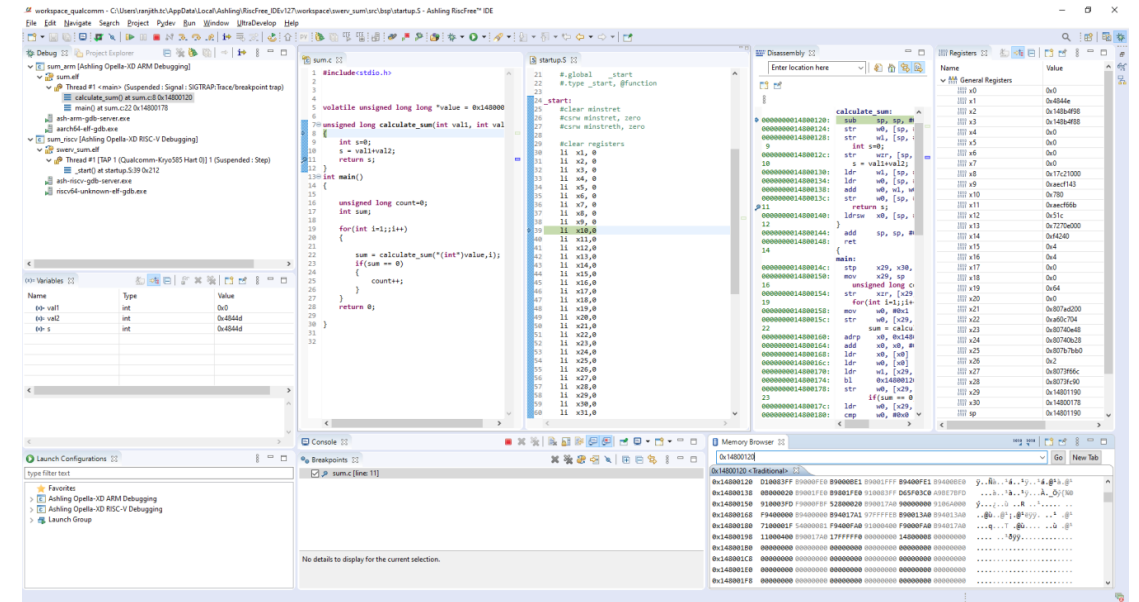
```
160 {
161     /* count the number of CLA/INS pairs found */
162     num++;
163     if (NULL == pApuFound)
164     {
165         /* store only first occurrence */
166         pApuFound = pAPDU;
167     }
168 }
169
170 /* get next table entry */
171 pAPDU = gpholAPDULib_Table[++i];
172 }
173
174 if ( PHOL_APDU_CLASS_NOT_FOUND == bClaFound )
175 {
176     /* no APDU found with that Class */
177     PHOL_APDU_SECURE_CALL( pholAPDU_Lookup ); // PRQA S 0309
178     return PHOL_APDU_ERROR_CLASS_NOT_SUPPORTED;
179 }
```



Accumulated Count	Accumulated Time	Average Time	Minimum Time	Maximum Time
0				1e+02
pholApu_PholApu_SECURE_CHECK		32		
phdCrc_PhdCrc_CRC_CALCULATECHECKSUM		21		
phdUart_PhdUart_UART_SETRECEIVEMODE		21		
phdUart_PhdUart_TXLASTBYTE		21		
phiso7816T1TX07816T1_SENDBLOCK		17		
phiso7816T1TX07816T1_TXSTATEMACHINE		17		
phEvalOs_KernelPHEVALOS_KERNEL		16		
phEvalOs_KernelPHEVALOS_MODEHANDLER		16		
phEvalOs_Loal_RestrictedPHEVALOS_RESTRICTEDMODE		16		
phiso7816L4PHISO7816L4_PARSEBYTES		16		

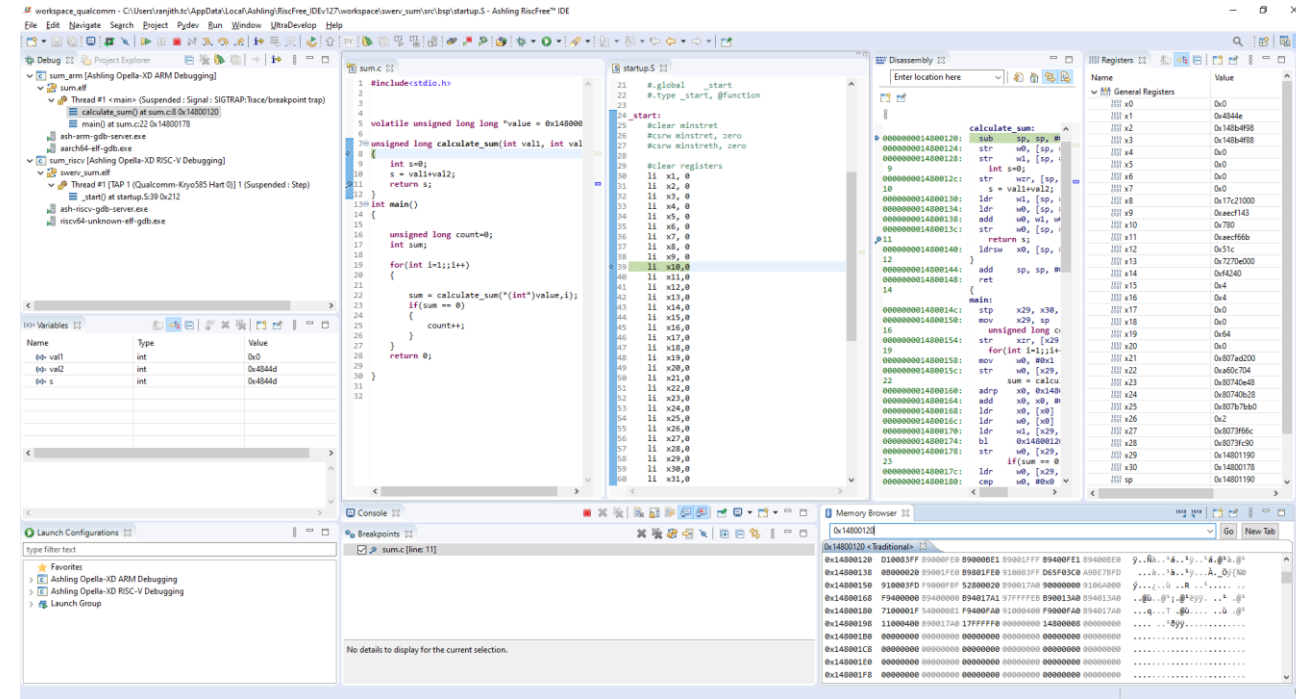
CORE-V IDE

- **CORE-V IDE** is a freely available, open-source development environment created by the OpenHW group
- Eclipse based IDE for CORE-V development
- Includes the Compiler Toolchain for CORE-V provided by Embecosm
- OpenOCD Debug Support
- “Ready-to-run” examples for Digilent boards
- Getting started guide
- Available end September 2020

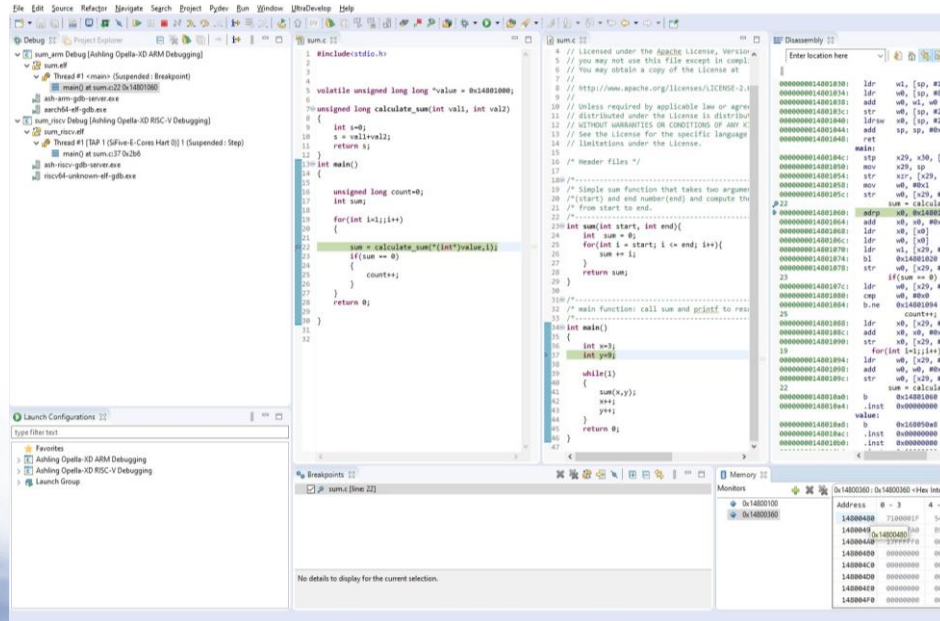


RiscFree IDE

- **RiscFree™** is Ashling's professional, commercial grade software development environment
- Supports a range of 32-bit and 64-bit devices
- Code-coverage analysis
- Profiling and Performance Analysis
- OS Debug support
- Multi-core Debug Support for homogeneous and heterogeneous debugging (e.g. RISC-V and non RISC-V)



RiscFree support for OpenHW CORE-V



RiscFree Eclipse based IDE + Opella-XD JTAG Probe + Genesys2 FPGA Board
Professional, commercial grade software development and debug environment

CORE-V Demo by Rejeesh S.B.

- CORE-V Demo using Ashling's **RiscFree** + Opella-XD Probe + Genesys2 FPGA platform
- How to build a CORE-V example program
- How to launch a Debug session using Opella-XD connected to the Genesys2 board
- Run-time debug features including go/stop/step/breakpoints and target access